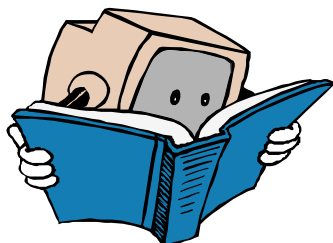


# HITACHI

**No. 0238**

**15LD2550B  
15LD2550EB**



**SERVICE MANUAL  
MANUEL D'ENTRETIEN  
WARTUNGSHANDBUCH**

**CAUTION:**

Before servicing this chassis, it is important that the service technician read the Safety Precautions and Product Safety Notices in this service manual.

**ATTENTION:**

Avant d'effectuer l'entretien du châssis, le technicien doit lire les «Précautions de sécurité» et les «Notices de sécurité du produit» présentés dans le présent manuel.

**VORSICHT:**

Vor Öffnen des Gehäuses hat der Service-Ingenieur die „Sicherheitshinweise“ und „Hinweise zur Produktsicherheit“ in diesem Wartungshandbuch zu lesen.

Data contained within this Service manual is subject to alteration for improvement.

Les données fournies dans le présent manuel d'entretien peuvent faire l'objet de modifications en vue de perfectionner le produit.

Die in diesem Wartungshandbuch enthaltenen Spezifikationen können sich zwecks Verbesserungen ändern.

**SPECIFICATIONS AND PARTS ARE SUBJECT TO CHANGE FOR IMPROVEMENT**

**Colour Television  
November 2007**

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# TABLE OF CONTENTS

<b>1. INTRODUCTION</b>	<b>3</b>
1.1. Purpose	3
1.2. Scope	3
1.3. General Features	3
<b>2. GENERAL DESCRIPTION</b>	<b>6</b>
2.1. Introduction	6
2.2. System Building Blocks	6
2.2.1. Analog Front End	6
2.2.2. Back End	6
2.2.3. General Block Diagram	7
2.2.4. Side Board(s)	8
2.3. Power Management	11
<b>3. APPENDIX</b>	<b>13</b>
3.1. Definitions, Acronyms and Abbreviations	13
3.2. Basic Components	17
3.2.1. VCTI	17
3.2.2. TSU 3XAWL	20
3.2.3. 74HC4052	22
3.2.4. 74HC4053	23
3.2.5. TDA2822M	23
3.2.6. LM1117	24
3.2.7. KA78L08	24
3.2.8. IRF7314	25
3.2.9. NTGS 3446	25
3.2.10. FDC642P	26
3.3. Board Connectors, Headers & Jumpers	26
3.3.1. Scart Connector1	27
3.3.2. PC Connector-	27
3.3.3. DVB Connector	28
3.3.4. Side A/V Connector	28
3.3.5. IDTV_IF Connector	29
3.3.6. Led Connector without MECH SW	29
3.3.7. Led Connector with MECH SW	29
3.3.8. Keypad Connector	29
3.3.9. MSTAR Debug Connector	29
3.3.10. Flash Prog. And VCTI Debug Connector	30
3.3.11. LVDS Panel Connector	30
3.3.12. Speaker Right Audio Out	30
3.3.13. Speaker Left Audio Out	30
3.3.14. Side Headphone Connector	31

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## 1. Introduction

### 1.1. Purpose

The purpose of this document is to define the DHDS and the operation of 17MB21, 15"XGA with LVDS input, 19" SXGA with double LVDS input. It is aimed to provide information to engineering staff to understand the operation and specs of the TV.

The other related technical documents are as follows:

	Title:
1	17MB21 Schematics
2	IR Receiver and Led Display Board Schematics
3	Keypad Board Schematics
5	VCTI49xy Datasheet –( Video-Controller-Text-IF-Audio IC)
6	TSU33AWL for 15"XGA TSU36AWL for SXGA Datasheet –( Controller with Analog Interface and Multi-Purpose Output Transmitter)
7	Other ICs Datasheets (Please check the table in Appendix 3.2 for the complete component list.).

**Table : Related documents.**

### 1.2. Scope

The document covers detailed descriptions of 17MB21 chassis system building blocks.

### 1.3. General Features

General product specifications and overview of the system will be introduced in this part. The system is a low end; 15" and 19" TFT LCD TV solution basically for EU market with VCTI49XYI and TSU33AWL or TSU36AWL Video Image Processor chip-set on single-layer PCB. As the first target market is EU, the first release of the TV will support PAL/SECAM B/G/D/K/I/L/L'.

#### **The other general default features of the TV are as listed below:**

- IR Control (RC5 and other customer specific protocols)
- OSD
- 100 Program Storage Locations
- Teletext
- No Ident Timer
- Screen Size (15", 19")
- Child Lock
- Sleep Timer
- 170/270V AC Plug
- ST-BY Power Consumption <1W
- 1 Scart input (1<sup>st</sup> Full)
- S-VHS Input , BAV input
- 75 ohms antenna input
- PC Input (VGA)
- 2H/4H Comb Filter

---

## **Sound Features**

- Equalizer
- FM Radio
- Linear Stereo
- German-NICAM Stereo
- 5 Band Equalizer Control
- SRS TRU Surround (OPT)
- SRS TRU Bass (OPT)
- BBE, WOW (OPT)
- Stereo Audio Output Power (2x2W )
- 16R speaker
- Volume Controlled HP Output, Stereo Audio line out, Stereo Audio line in
- Coaxial Audio Output (with IDTV or DVD Option)
- Detachable Headphone Output (OPT)

## **Picture**

- 4:3 PANEL --- 4:3, 16:9, Auto
- Picture Modes (Bright, Standard, Soft)
- Media Window Enhancement (MWE)
- White balance settings (warm/normal/cool) for TV&PC
- Auto Shut down
- Multi System Reception : PAL-SECAM BG-DK-I/I'-L/L'
- NTSC Video Playback
- WSS (16:9 / 4:3 Aspect Ratio Auto Switch)
- Channel Type Sorting (Favorite/Sport/Music/News/Movie)

## **Tuning**

- FST
- Frequency Search (OPT)
- APS (Auto Search / Name / Sort)
- Auto Search
- CATV / HYPERBAND

## **Keyboard**

- Volume -/ +Button
  - Program -/+ Button
  - Menu Button
  - TV / AV Button
  - Teletext/OSD
  - Simple Text 10 Pages
  - Fastext & Top Text (OPT)
  - Teletext Languages (ALL)
  - Character Based OSD
  - OSD Color & Transparency Selection
-

---

**The general optional features of the system are as listed below:**

- AV Input
- Y/Pb/Pr support via VGA connector
- Full Green Mode DPMS Support
- Plug & Play (DDC2Bi) For Windows 9X, ME, 2000, XP (OPT)
- Headphone {side || on board} (When the headphone is used, TV volume cut off automatically)
- IDTV With Single CI Connector (OPT)
- DVD (OPT)
- Comb Filter (OPT)
- LTI, CTI (OPT)
- IDTV
- OSD: 22 Menu Languages ENG, FRA, GER, ITA, SPA, POR, TUR, SWE, DEN, FIN, NOR, POL, HUN, CZE, BUL, ROM, RUS, DUTCH, CRO, SLOVAK, SLOVENIAN and GRE.
- 2x2W Speaker Output Power.

---

## 2. General Description

### 2.1. Introduction

This chapter describes system building blocks in detail.

### 2.2. System Building Blocks

17MB21 chassis main blocks are as follows:

- **Analog Front End** : VCTI (Microcontroller + Video Processor + Sound Processor + IF+ Keyboard/IR Interface+OSD), Audio Amp.
- **Back End** : TSU33AWL or TSU36AWL (Scaler, Deinterlacer, OSD generator, LVDS transmitter)
- **Side Board(s)** : Keyboards, IR/LED Boards, FAV Boards, Headphone Boards.

#### 2.2.1. Analog Front End

17MB21 Main Board consists of two major blocks. The first block is analog front-end and this block is handled by VCTI chip that is highly multifunctional. This IC does demodulation of Video & Audio from Tuner IF, CVBS, Audio, RGB, SVHS input selection and processing. It has an audio processor that supports equalizer or tone control, volume control, AVL, surround effect etc and supplies amplifier, headphone and CVBS & audio line outputs. It handles video processing such as colour standard detection and demodulation, picture alignment (brightness, contrast, colour etc.). The IC also does teletext decoding with fastext memory. After video processing, the processed video is applied to TSU3XAWL chip in RGB format.

The TV Tuner is an asymmetrical or a symmetrical IF output type and is PLL controlled. The IF signal is applied single saw filter. After the SAW filter block, IF signal is applied to VCTI IF inputs (Pin 16 and 17).

As VCTI can handle all the audio processing, there is no need for additional audio processor solution on the board. VCTI supports three Audio outputs. These outputs are assigned to Line-out, Speaker and SC1 audio out. The board employs TDA2822M to drive speakers and headphone.

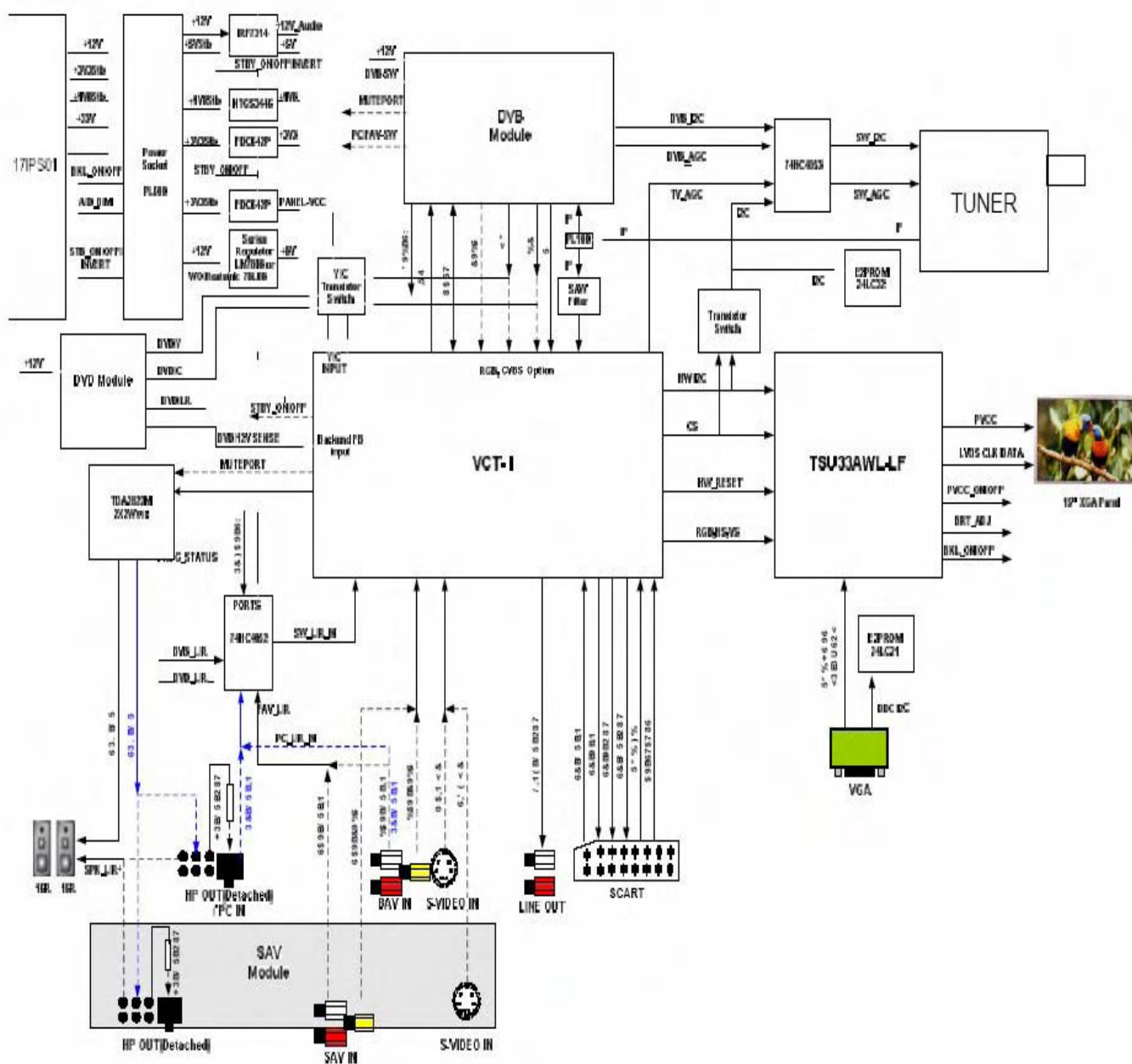
#### 2.2.2. Back End

The Back End section is handled by TSU chip. The RGB input can handle standard interlaced RGB output from VCTI, PC VGA RGB input and YPbPr. There are two set of ADC is present in TSU which are assigned to YPbPr/VGA and VCTI RGB output sources.

TSU33AL chip have an integrated 6/8-bit LVDS transmitter.

Backlight dimming and Panel power supply On/Off control is achieved via TSU chip. There are two pins to control inverter one of them is used for adjusting backlight the other one is used for backlight on/off control. Backlight on/off control is performed by VCTI.

### 2.2.3. General Block Diagram



### Figure 1

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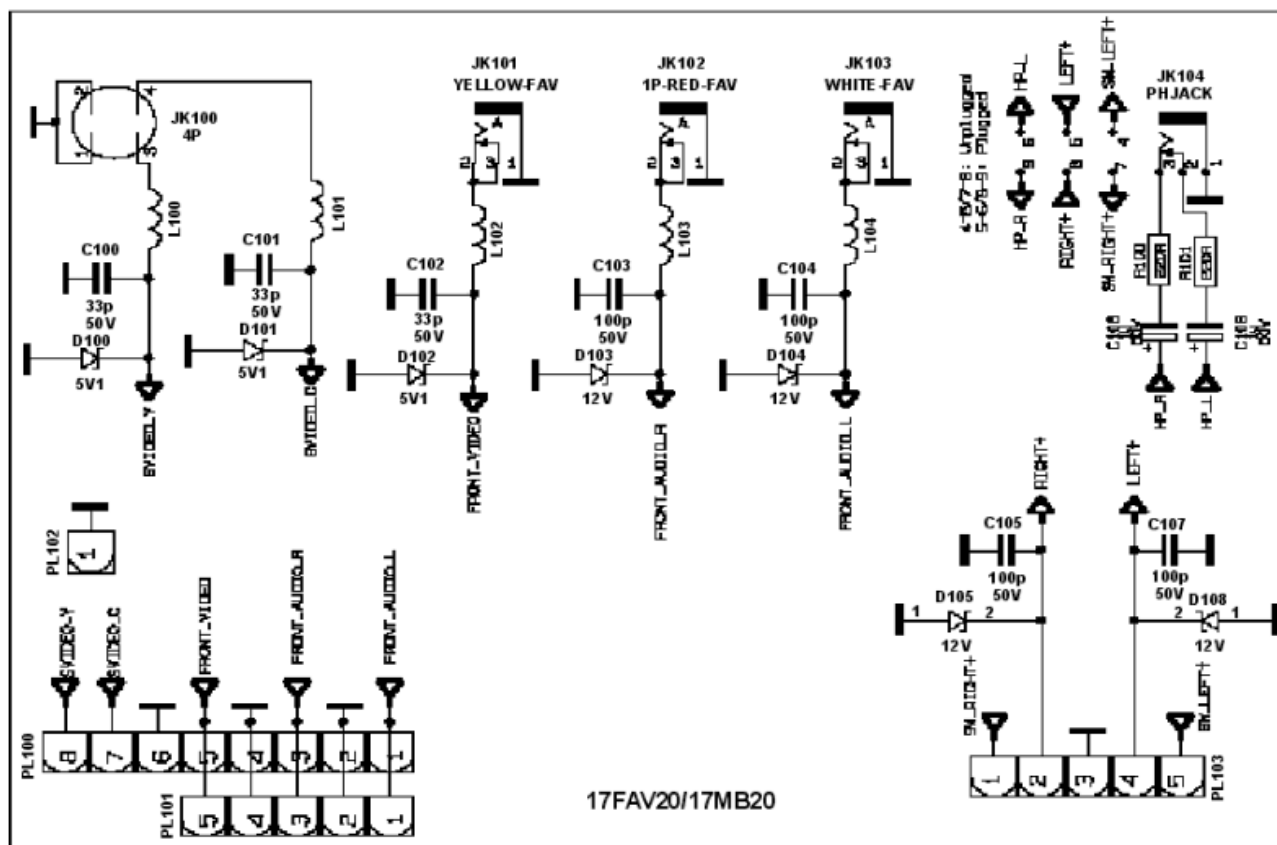
## 2.2.4. Side Board(s)

### 2.2.4.1. Side Audio Video

Front Audio Video board (17FAV20) for 17MB21 main board is detailed in the Table below.

Connector Name	Type	Function
JK100	SVHS Jack 4P DIN Type	Side SVHS Input
JK101	RCA Jack Yellow	Side CVBS Input
JK102	RCA Jack Red	Side Audio Input Right
JK103	RCA Jack White	Side Audio Input Left
JK104	Headphone Jack	Side Headphone
PL100	Connector Header 8P	Connector 8P for SVHS
PL103	Connector Male 5P	Connector 5P for HP
PL101	Connector Male 5P	Connector 5P for CVBS, Audio R and L





#### 2.2.4.2. Keypads

The keypads button descriptions for 17MB21 main board are listed in the Table below.

Key Name	Type	Function
Power*	Soft sw.	Power shut-down and turn on
Stand-by*	Tact sw.	Switch between stand-by and turn on modes.
TV/AV	Tact sw.	Input source select button.
Menu	Tact sw.	Display main menu on the screen. If any menu is active, display the upper menu. If main menu is active, turn menu off.
Program-	Tact sw.	Go to the lower program at any time in TV mode. (Scroll key function in menu mode)
Program+	Tact sw.	Go to the upper program at any time in TV mode. (Scroll key function in menu mode)
Volume-	Tact sw.	Decrease the volume level in the volume. (Scroll key function in menu mode)
Volume+	Tact sw.	Increase the volume level in the volume. (Scroll key function in menu mode)

\*In any T.V. set only one of them can be used.



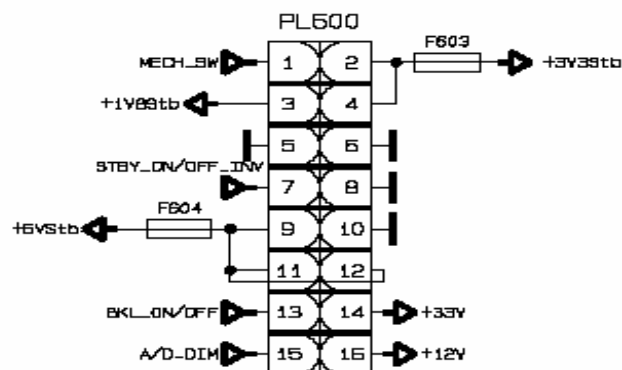
## 2.3. Power Management

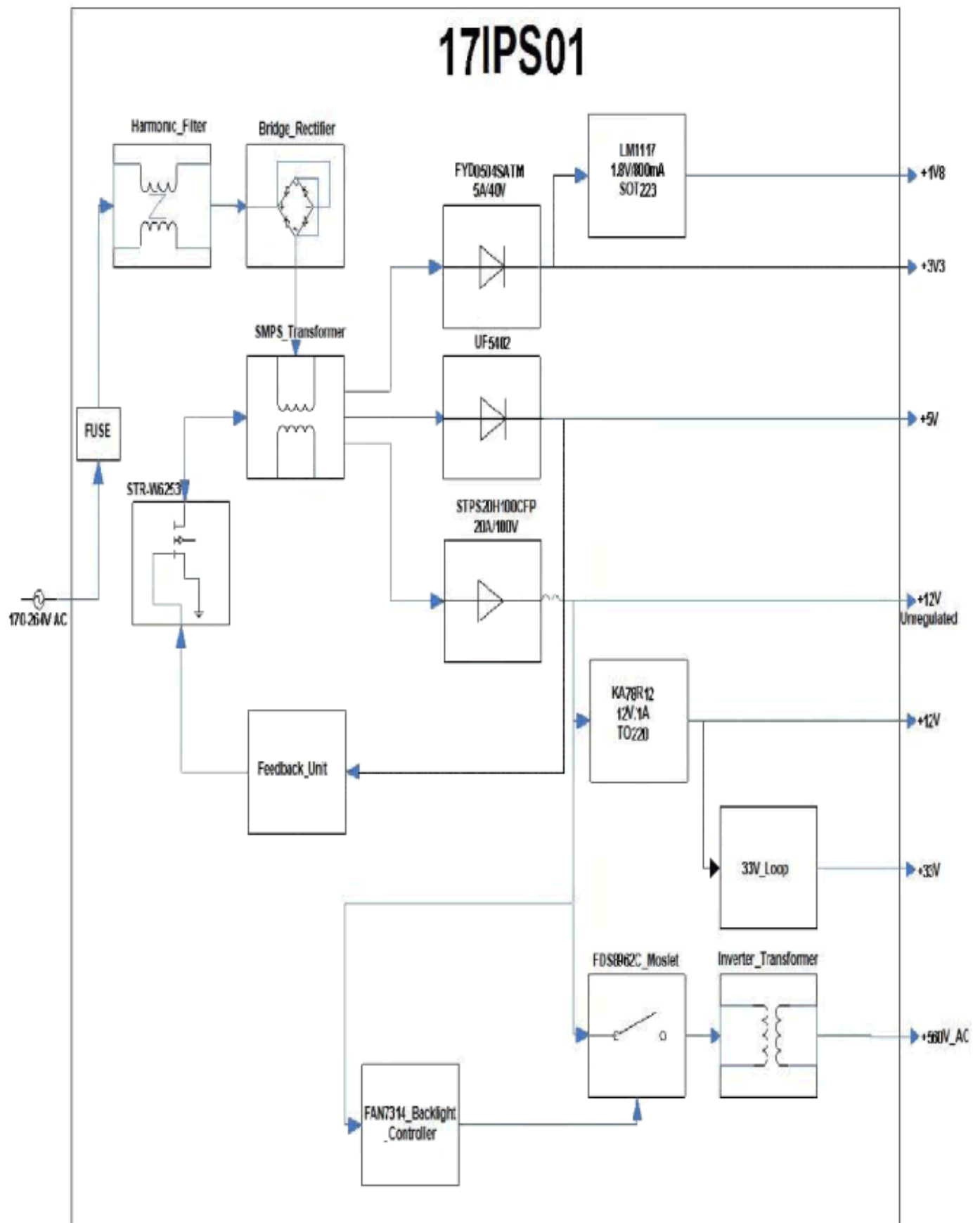
All power requirements supplied from LIPS (Light Integrated Power Supply) Boards.  
IPS01 Lips Board used for 15" products and IPS02 for 19" products.  
(Please check the Table below for power management details.)

Main Board Requirements	
Voltage	Max Current
+33V	5mA
+12V_AUD	200mA
+8V	12mA
+5V	160mA
+3V3	370mA
+1V8	220mA
+12VStb	30mA
+5VStb	30mA
+3V3Stb	205mA
+1V8Stb	400mA
Panel Logic Cct Requirements	
Voltage	Max Current
+3V3	1100mA
+5V	1200mA

**Table : Power management table.**

PL600 socket is used for power connections.





**Figure 3: IPS01 Block Diagram**

17IPS01 Outputs	
Voltage	Current
+33V	5mA
+12V_Unregulated	1000mA
+12V	700mA
+5V	300mA
+3V3	1600mA
+1V8	400mA
+560V_AC	15mA

---

### **3. APPENDIX**

#### **3.1. Definitions, Acronyms and Abbreviations**

2CS	Dual Carrier Stereo a.k.a. German Stereo.
ACI	Automatic Channel Installation,
ACL	Automatic Colour Limiting
ADC	Analogue to Digital Converter
AF	Audio Frequency
AFC	Automatic Frequency Control
AGC	Automatic Gain Control
AKB	Auto Kine Biasing
API	Application Programmers Interface.
ASD	Automatic Standard Detection
ASP	Audio Signal Processor (on Picasso)
ATS	Automatic Tuning System,
AV	External Audio and Video TV peripheral.
AVC	Audio Video Control
AVL	Automatic Volume Leveling
BBE	Bass enhancement licensed by BBE Inc.
BE	Back-End
BKS	Black Stretch
BTSC	Broadcast Television Systems Committee USA standard
CC	Closed Captioning.
CCC	Continuous Cathode Calibration
CE	Configuration Element
CLUT	Colour Look Up Table
COR	Contrast Reduction
CVBS	Combined Video, Blanking and Sync.
DAC	Digital to Analogue Converter
DBE	Dynamic Bass Enhancement
DDEP	DEMDEC Easy Programming; operation mode of DEMDEC.
DEMDEC	Stereo demodulator decoder; part of ASP.
DPL	Dolby Pro Logic
DPTR	Data PoinTeR
DRCS	Dynamically Redefinable Character Set.
DSP	Digital Signal Processor (or Processing)
DUB	Dynamic Ultra Bass
EPG	Electronic Program Guide.
FA	Factory mode
FASTEXT	Special way of accessing teletext pages
FB	Fast Blanking
FE	Front End
FLOF	Full Level One Features (synonym for Fastext)
FST	Frequency Synthesis Tuning

---

GTV	Global TeleVision.
HP	Headphone
HSH	Horizontal Shift
IF	Intermediate Frequency. Normally the output of the tuner.
IIC	Inter Integrated Circuit
IIS	Inter Integrated Sound
LibCoMa	Library Configuration Manager.
LS	Loudspeaker
MIPS	Million Instructions Per Second
MPX	Japanese multiplexed sound standard
MS	Multi Standard
NICAM	Near Instantaneously Compacted Audio Multiplex
NTSC	National Television System Committee. Colour encoding system.
NVM	Non-Volatile Memory
OSD	On Screen Display
OSRP	Overall System Realization Process
OTP	One Time Programmable
PAL	Phase Alternating LineColour encoding system.
PAT	Painter Authoring Tool. Development support tool to define Painter character sets (and UIMS data structures).
PB	Picture Booster
PIP	Picture In Picture
PLL	Phase Locked Loop
PMT	Power Management
PP	Personal Preferences
PS-MTS	Mainstream Television Solutions
PSW	Program Status Word
PWM	Pulse Width Modulation
RC-5	Remote Control system
RCP	Remote Control Preprocessor
RF	Radio Frequency TV signal broadcast.
RGB	Red, Green Blue. The colour signals.
Round-robin	A style of scheduling where each task is executed in turn, provided it is ready to run.
RPMS	Resource Persistent Memory Store
RTC	Real Time Clock
SAP	Second Audio Program; part of BTSC sound system.
SAW	Surface Acoustic Wave
SCART	External CVBS, S-VHS and Sound input/output, RGB and switching input.
SCI	Software Configuration Item
SCL	Serial Clock
SDA	Serial Data
SDE	Software Development Environment
SECAM	Sequentiel a Memoire Colour encoding system.
Set-maker	The manufacturer/developer of the end product.
SFR	Special Function Register.
SHLD	Software High Level Design
SIF	Sound Intermediate Frequency
SRT	Signal RouTing
SS	Source Switching
SSS	Static Standard Selection

---

State	The condition of a component that results in a particular observable behaviour.
Status Handler	A step that handles a status change, by managing the response to the change.
STB	SetTop Box
TOP(TEXT)	Table Of Pages, Special way of accessing teletext pages
TXT	Teletext
UHF	Ultra High Frequency
UI	User Interface
UIMS	User Interface Management System
UOC	Ultimate One Chip
User	See Set-maker
VDS	Virtual Dolby Surround
VG2	Voltage at Gate 2
VHF	Very High Frequency
VIF	Video Intermediate Frequency
VOD	Video On Demand
VPS	Video Programming delivery control System
VS	Vertical Slope
VSH	Vertical Shift
VSP	Video Signal Processor (on Cosmic)
VST	Voltage Synthesis Tuning
Y/C	Luminance/Chroma signal, S-VHS
YprPb	Luminance Y and colour difference signals (Pr - red, Pb - blue, colour bar 100% saturation)
YUV	Luminance (Y) and colour difference signals (U and V).
<b>Audio Preset:</b>	Pre-defined audio reproduction settings stored in NVM. The values of the items in a Preset can be set in service.
<b>SCAVEM:</b>	SCAn VELOCITY Modulation
<b>User 1:</b>	User defined setting for height of a 16:9 picture setting
<b>User 2:</b>	User defined setting for the zoom and the scroll of a 16:9 picture setting
<b>Indicator:</b>	An on screen object, giving textual or graphical information on user commands or system events
<b>NVM:</b>	Non Volatile Memory, used to store user and service/factory settings
<b>Program:</b>	A broadcasted TV signal received via the tuner. A program can be identified by the frequency by which it is transmitted.
<b>Source:</b>	The selected input of the TV receiver. This can either be a the front end (i.e. a program) or an external AV source
<b>Video Preset:</b>	Pre-defined video reproduction settings stored in NVM. The values of the items in a Preset can be set in service.
<b>White tone:</b>	Pre-defined values for the white point RED, GREEN and BLUE settings. The values of the white point settings for each white tone setting can be set in service.
<b>Hue:</b>	Tint
<b>First/last program:</b>	0-99 for 100 programs available
<b>Available program:</b>	First available program is the lowest program number in NVM that is marked as <i>not skipped</i> . When all programs are skipped then the lowest program number is used. Last available program is the highest program number in NVM, which is marked as <i>not skipped</i> . When all program numbers are skipped then the highest program number is used.

---

<b>Program number:</b>	A program number identifies a location in NVM. At this location all program information, like frequency, lock, AFC, etc., can be found. Selecting a program invokes activating the program information.
<b>Last status:</b>	<p>A variable can be classified as 'last status' setting. Settings that are classified as 'last status' are stored in NVM. The following settings are part of the last status:</p> <ul style="list-style-type: none"><li>• Program number</li><li>• Volume</li><li>• Audio Preset</li><li>• Video Preset</li><li>• Aspect ratio</li></ul>
<b>WSS:</b>	Wide Screen Signalling
<b>Letterbox:</b>	When a 14:9 or 16:9 format movie or picture on 4:3 transmission displayed on 4:3 set, black bars on top and the bottom of the screen are displayed. This is called letterbox or 4:3 letterbox.

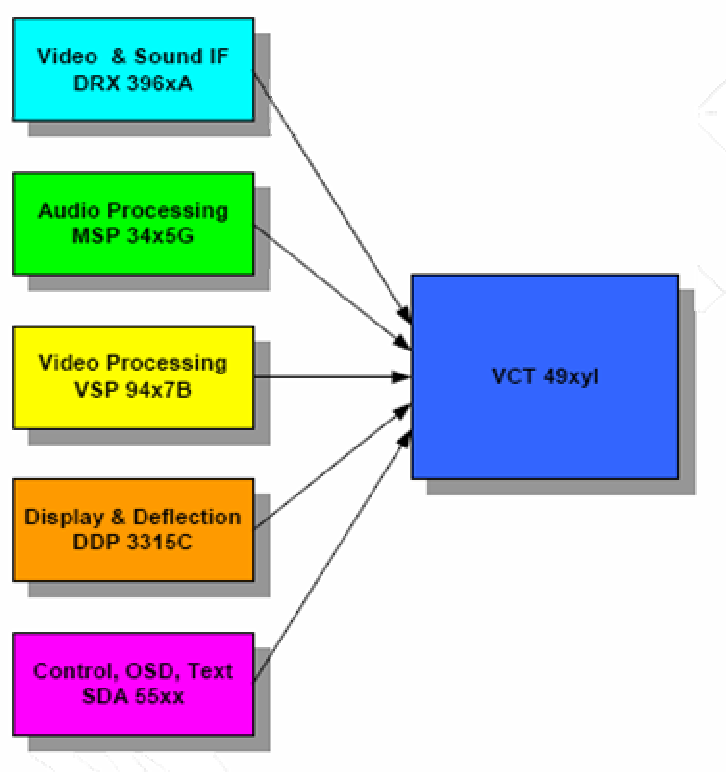


## 3.2. Basic Components

No	Title	Description	Supplier
	VCTI	Video-Controller-Text-IFAudio IC Family	Micronas
	TSU33AWL or TSU36AWL	XGA LCD controller with analog interface and Single(TSU33AWL)/Double(TSU36AWL) LVDS Transmitter	Mstar
	74HC4052	Dual 4- channel analog multiplexer/demultiplexer	Philips
	74HC4053	triple 2-channel multiplexer	Philips
	TDA2822M	Dual Low Voltage Power Amplifier	ST
	LM1117	800mA Low Dropout Linear Regulator	National Semiconductor
	KA78L08	3-Terminal 0.1A Positive Voltage Regulator	Fairchild
	IRF7314	Dual P-Channel Mosfet	IR
	NTGS3446	Single N-Channel Mosfet	On-Semi
	FDC642P	Single P-Channel Mosfet	Fairchild

### 3.2.1. VCTI

VCTI49xy is composed of microcontroller, video proccessor, display and deflection processor, sound proccessor and IF blocks as shown in below Figure .



Fig

VCTI49xyl family has two package types; PSSDIP88 and PMQFP144. PSSDIP88 package is chosen because of its compatibility for soldering in production. PSSDIP88 package has two

---

versions; 1 and 2. PSSDIP88-2 package is the "pinning mirrored" version of PSSDIP88-1 and is preferred to be used for layout compatibility.

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### 3.2.1.3. VCTI Port Allocation

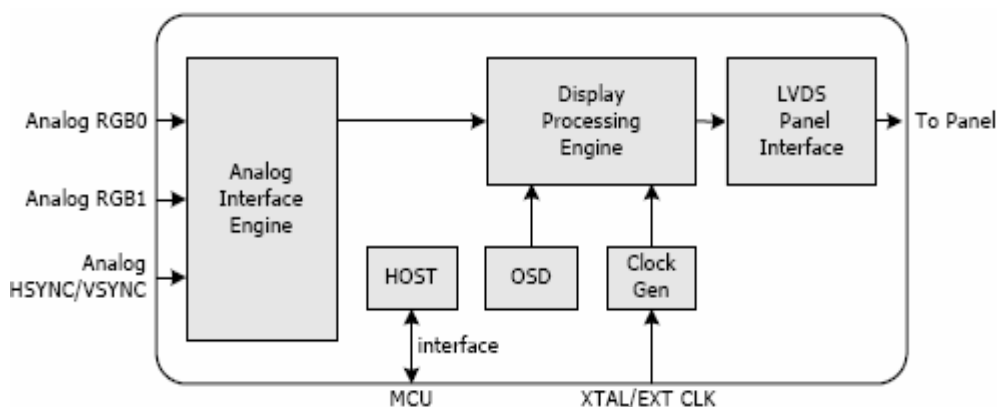
PIN NO	PORT NAME	SIGNAL NAME	TYPE	FUNCTION	NOTE
47	P10	HW RESET	O	Mstar reset	
48	P11	Rx/LED*	I/O	for IDTV communication/WO-IDTV	
49	P12	Tx/Led*	O	for IDTV communication/WO-IDTV	
50	P13	VCTI_VS	O	Vertical sync. output from vcti	
51	P14	Key	I	Keyboard function select	
52	P15	AV1_Status	I	Scart1 function select.	
53	P16	Program status	O	For 4052 Switch control	
54	P17	ON/OFF	O	Power switching signal	
55	P20	BKL_ON/OFF	O	Backlight on/off	
56	P21	CS	O	Communication between VCTI and Mstar	
62	Safety	VCTI_HS	O	Horizontal sync. output from vcti	
85	Vert+	IRQ	O	for IDTV communication	
27	P22	WP	O	Write protect for vcti	
28	P23	IR	I	Infrared Receiver	

\* This ports are used for different functionality according to IDTV support. In IDTV case Mute and Led functions are controlled by Digital Board.

## 3.2.2. TSU3XAWL

The TSU33AL is total solution graphics processing IC for LCD displays with panel resolutions up to XGA. It is configured with a high-speed integrated triple-ADC/PLL, a high quality display processing engine, and an integrated multi-purpose output display interface that can support LVDS panel interface formats. To further reduce system costs, the TSU33AL also integrates intelligent power management control capability for green-mode requirements and spread-spectrum support for EMI management.

### 3.2.2.1. Block Diagram



### 3.2.2.2. Pinout

### 3.2.2.3. PW1306 Port Allocation

PIN NO	PORT NAME	SIGNAL NAME	TYPE	FUNCTION	NOTE
36	PWM0	A/A_DIM	O	Backlight Brightness adjustment	
37	PWM1	PVCC_ON/OFF	O	Panel Supply Voltage On/Off	

### 3.2.3. 74HC4052

#### DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

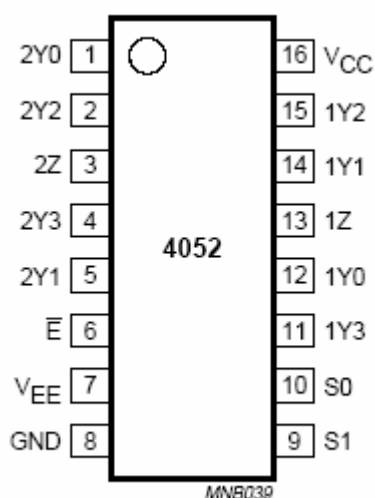
The 74HC4052 are dual 4-channel analog multiplexers or demultiplexers with common select logic. Each multiplexer has four independent inputs/outputs (pins nY0 to nY3) and a common input output (pin nZ). The common channel select logics include two digital select inputs (pins S0 and S1) and an active LOW enable input (pin  $\bar{E}$ ). When pin  $\bar{E}$ =LOW, one of the four switches is selected (low-impedance ON-state) with pins S0 and S1. When pin  $\bar{E}$ =HIGH, all switches are in the high-impedance OFF-state, independent of pins S0 and S1.

FUNCTION TABLE

INPUT <sup>(1)</sup>			CHANNEL BETWEEN
$\bar{E}$	S1	S0	
L	L	L	nY0 and nZ
L	L	H	nY1 and nZ
L	H	L	nY2 and nZ
L	H	H	nY3 and nZ
H	X	X	none

**Note**

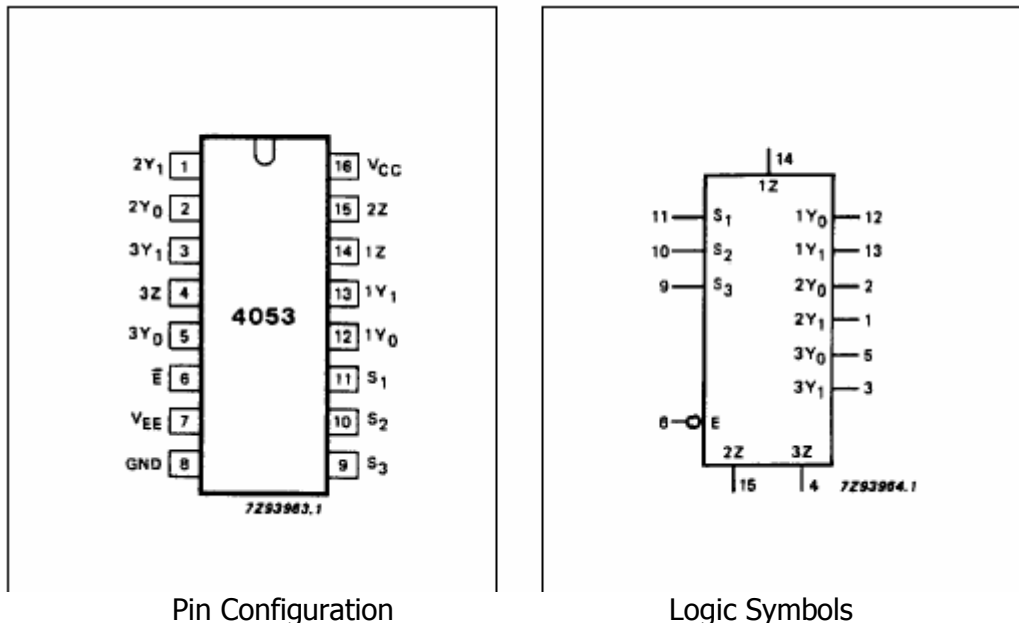
1. H = HIGH voltage level  
L = LOW voltage level  
X = don't care.



Pin Configuration

### 3.2.4. 74HC4053

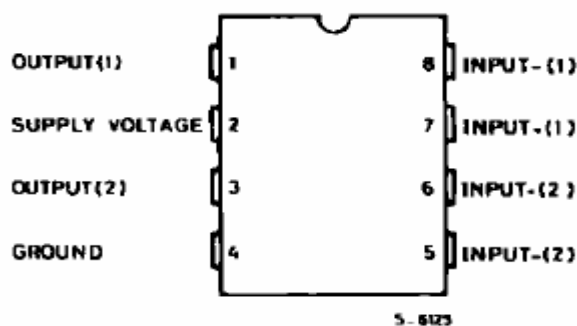
74HC4053 are triple 2-channel analog multiplexers/demultiplexers with a common enable input ( $\bar{E}$ ). Each multiplexer /demultiplexer has two independent inputs/outputs ( $nY_0$  and  $nY_1$ ), a common input/output ( $nZ$ ) and three digital select inputs ( $S_1$  to  $S_3$ ). With  $\bar{E}$  LOW, one of the two switches is selected (low impedance ON-state) by  $S_1$  to  $S_3$ . With  $\bar{E}$  HIGH, all switches are in the high impedance OFF-state, independent of  $S_1$  to  $S_3$ .

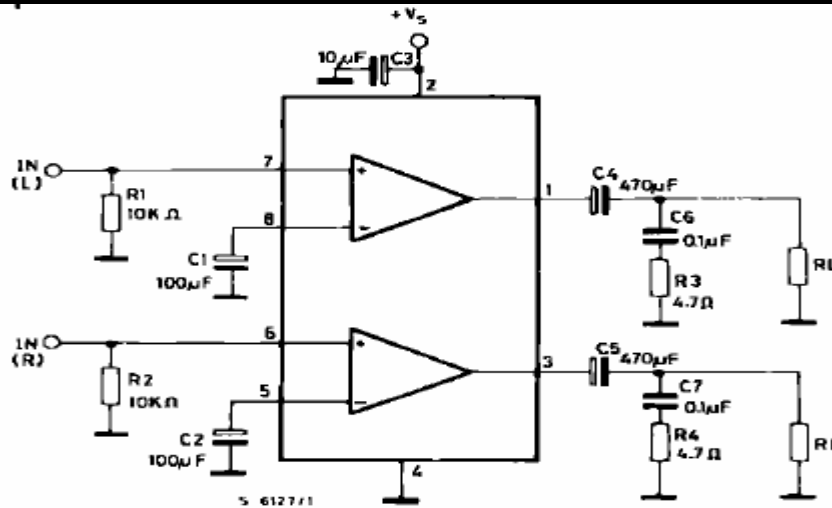


### 3.2.5. TDA2822M

## Dual Low Voltage Power Amplifier

TDA 2822M is a monolithic integrated circuit in 8 lead Minidip package. It is intended for use as dual audio power amplifier.



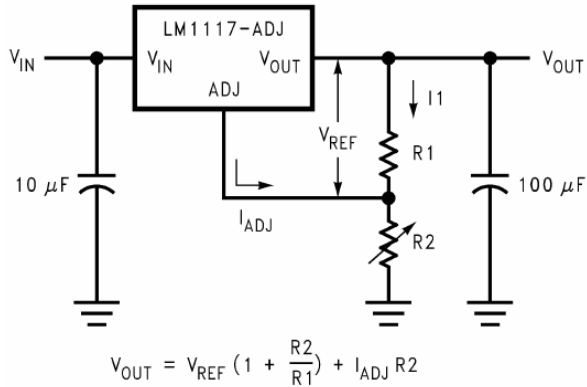


Stereo Test Circuit

### 3.2.6. LM1117

The LM1117 is a series of low dropout voltage regulators with a dropout of 1.2V at 800mA of load current.

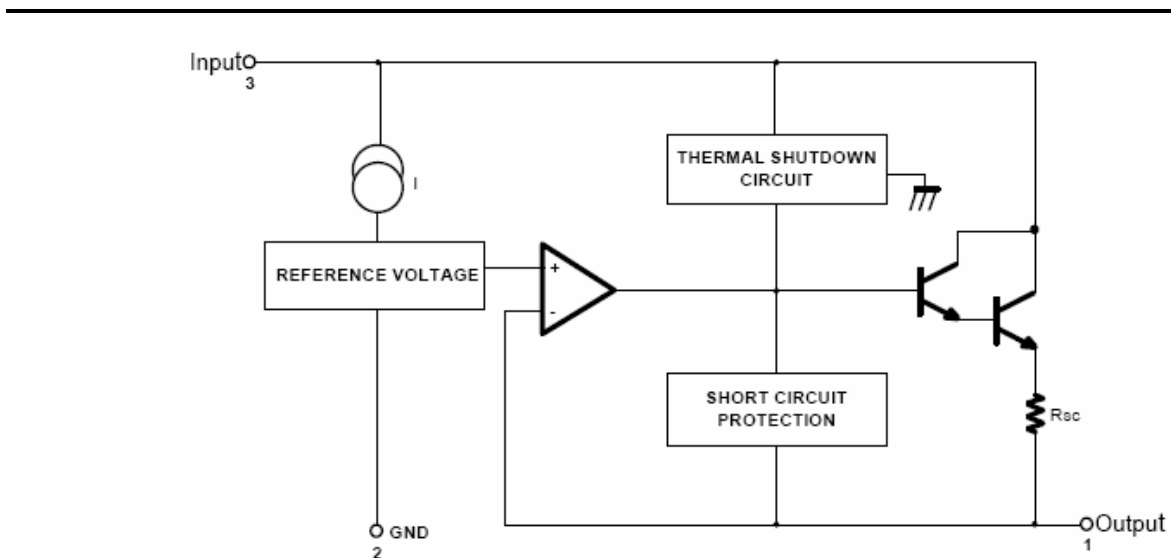
The LM1117 is available in an adjustable version, which can set the output voltage from 1.25V to 13.8V with only two external resistors. In addition, it is also available in five fixed voltages, 1.8V, 2.5V, 2.85V, 3.3V, and 5V. The output voltage is adjusted according to the formula shown in Figure



### 3.2.7. KA78L08

KA78LXXA series of fixed voltage monolithic integrated circuit voltage regulators are suitable for application that required supply current up to 100mA.





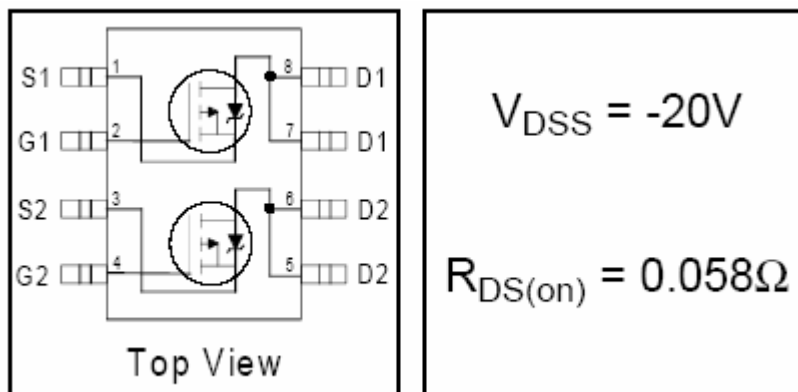
KA78LXX Internal Block Diagram

### 3.2.8. IRF7314

Dual P-Channel Mosfet.

\*Extremely Low On-Resistance

\*Fast Switching Speed



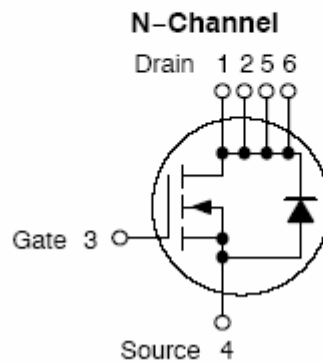
### 3.2.9 NTGS 3446

N-Channel Mosfet

\*Ultra Low  $R_{DS(on)}$

\*Fast Switching Speed

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
20 V	36 m $\Omega$ @ 4.5 V	5.1 A



### 3.2 10 FDC642P

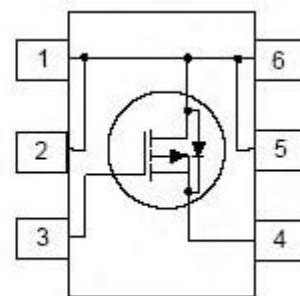
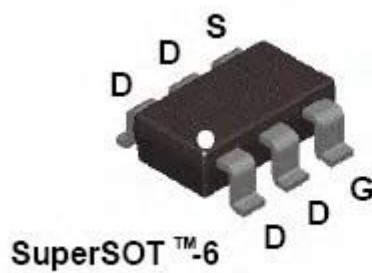
P-Channel Mosfet

\*Ultra Low  $R_{DS(ON)}$

\* Fast Switching Speed

\* Low Gate Charge

- -4 A, -20 V.  $R_{DS(ON)} = 0.065 \Omega$  @  $V_{GS} = -4.5$  V  
 $R_{DS(ON)} = 0.100 \Omega$  @  $V_{GS} = -2.5$  V



### 3.3. Board Connectors, Headers & Jumpers

### 3.3.1. Scart Connector1 (PL301)

Pin	Signal	Description	Signal level	Impedance
1	SC1_R_OUT	Audio output (right)	0.5V rms	<1kohm
2	SC1_R_IN	Audio input (right)	0.5V rms	>10kohm
3	SC1_L_OUT	Audio output (left)	0.5V rms	<1kohm
4		Ground (audio)	-	-
5		Ground	-	-
6	SC1_L_IN	Audio input (left)	0.5V rms	>10kohm
7	SC1_B	Blue input	0.7V	75ohms
8	AV1_STATUS	Function select AV control)	High (9.5-12V) - AV mode Mid (5-8V) - Wide-screen Low (0-2V) - TV mode	>10kohm
9		Ground	-	-
10	SDA	For flash update	Digital	-
11	SC1_G	Green input	0.7V	75ohms
12	SCL	For flash update	Digital	-
13		Ground (red)	-	-
14		Ground (blanking)	-	-
15	SC1_R	Red input or Chrominance input	0.7V / 0.3V	75ohms
16	SC1_IN_FB	RGB switching control	High (1-3V) - RGB Low (0-0.4V) - Composite	75ohms
17		Ground (video input & output)	-	-
18		Ground (RGB switching control)	-	-
19	SC1_V_OUT	Video out (composite)	1V including sync	75ohms
20	SC1_V_IN	Video input (composite) or Luminance input	1V including sync	75ohms
21		Common ground (shield)	-	-

### 3.3.2. PC Connector-(1x15 PL303)

Pin #	Logic	I/O	Signal Description	Signal Level	Impedance
1	Analog	I	Red Component		75Ω
2	Analog	I	Green Comp.		75Ω
3	Analog	I	Blue Comp.		75Ω
13	TTL	I	Horizontal Sync		
14	TTL	I	Vertical Sync		
12	TTL	I/O	I2C Data		
15	TTL	I	I2C Clock		
9	Power	I	+5V		
4,5,6,7,8,10	Ground				
11	No Connect				

---

### 3.3.3. DVB Connector (2x12 PL302)

Pin	Symbol	Description
1	DVB_IN_R	DVB Red Signal
2	GND	Ground
3	DVB_IN_G	DVB Green Signal
4	GND	Ground
5	DVB_IN_B	DVB Blue Signal
6	GND	Ground
7	DVB_IN_CVBS	DVB Video Signal
8	GND	Ground
9	DVBL	Digital Sound Left
10	DVBR	Digital Sound Right
11	GND	Ground
12	GND	Ground
13	AGC_DVB	DVB AGC Signal
14	LEDCON	Led Control Port
15	DVB_SW	DVB Sound Switch port
16	Muteport	Mute Control Port
17	N.C.	N.C.
18	RXD	Receive
19	TXD	Transmit
20	IRQ	Interrupt Request
21	GND	Ground
22	GND	Ground
23	SDA_DVB	DVB Data Signal
24	SCL_DVB	DVB Clock Signal

### 3.3.4. Side A/V Connector (1x8 PL304)

Pin	Signal	Description	Signal level	Impedance
1	FAVINL	Audio in (left)	0.5V rms	>10kohm
2	Gnd	Ground (audio)	-	-
3	FAVINR	Audio in (right)	0.5V rms	>10kohm
4	Gnd	Ground (audio)	-	-
5	CVBS_IN	Function select (AV control)	1V including sync	75ohms
6	Gnd	Ground (audio)		
7	SVHS_C	Chroma input	0.7V	75ohms

Pin	Signal	Description	Signal level	Impedance
8	SVHS_Y	Luma input	0.7V	75ohms

### 3.3.5. IDTV\_IF Connector (1x3 PL100)

Pin	Signal
1	IF2
2	IF1
3	Gnd

### 3.3.6. Led Connector WO/MECH SW(1x5 PL101)

Pin	Signal	Description
1	GND	Ground
2	3v3_STB	3.3 V Standby
3	5V	ON/OFF
4	IR	Infrared
5	VIN	Supply

### 3.3.7. Led Connector W/MECH SW(1x6 PL102)

Pin	Signal	Description
1	MECH_SW	Mechanic Switch
2	GND	Ground
3	3v3_STB	3.3 V Standby
4	5V	ON/OFF
5	IR	Infrared
6	VIN	Supply

### 3.3.8. Keypad Connector(1x4 PL103)

Pin	Signal	Description
1	GND	Ground
2	KEY	AV Tact SW
3	Soft SW	Soft SW
4	KEY	Program and Volume SW

### 3.3.9. MSTAR Debug Connector (1x4 PL105)

Pin	Signal	Description
1	RXD	Receive
2	TXD	Transmit
3	GND	Ground
4	5V	5 Volt

---

### 3.3.10. Flash Prog. And VCTI Debug Connector (1x5 PL104)

Pin	Signal	Description
1	5V	ON/OFF
2	KEY	Key signal
3	GND	Ground
4	HWSDA	Data signal (VCTI side)
5	HW_SCL	Clock signal (VCTI side)

### 3.3.11. LVDS Panel Connector(2x10 PL403)

Pin	Symbol	Description
1	PVCC	Panel Voltage
2	TXOUT3+	LVDS Signal(+)
3	PVCC	Panel Voltage
4	TXOUT3-	LVDS Signal(-)
5	V3_3D or LVDS_GND	+3.3V or Ground
6	TXCLKOUT+	LVDS Signal(+)
7	LVDS_GND	Ground
8	TXCLKOUT-	LVDS Signal(-)
9	LVDS_GND	Ground
10	TXOUT2+	LVDS Signal(+)
11	LVDS_GND	Ground
12	TXOUT2-	LVDS Signal(-)
13	LVDS_GND	Ground
14	TXOUT1+	LVDS Signal(+)
15	LVDS_GND	Ground
16	TXOUT1-	LVDS Signal(-)
17	LVDS_GND	Ground
18	TXOUT0+	LVDS Signal(+)
19	LVDS_GND	Ground
20	TXOUT0-	LVDS Signal(-)

### 3.3.12. Speaker Right Audio Out (1x2 PL500)

Pin	Signal
1	Right+
2	Right -

### 3.3.13. Speaker Left Audio Out (1x2 PL501)

Pin	Signal
1	Left+
2	Left -

---

### 3.3.14. Side Headphone Connector (1x5 PL502)

Pin	Signal	Description
1	Right+ IN	Right sound input for HP
2	Right+ Out	Right sound output for HP
3	GND	Ground
4	Right+ Out	Right sound output for HP
5	Right+ IN	Right sound input for HP

### 3.3.15 DVD Audio Connector (1x6 PL308)

Pin	Signal	Description
-	DVD_L	DVD Audio Left
2	GND	Ground
3	DVD_R	DVD Audio Right
4	GND	Ground
5	DVD_SENSE	DVD On Sense
6	DVD_IR	DVD IR Signal

### 3.3.16 DVD Video Connector (1x3 PL307)

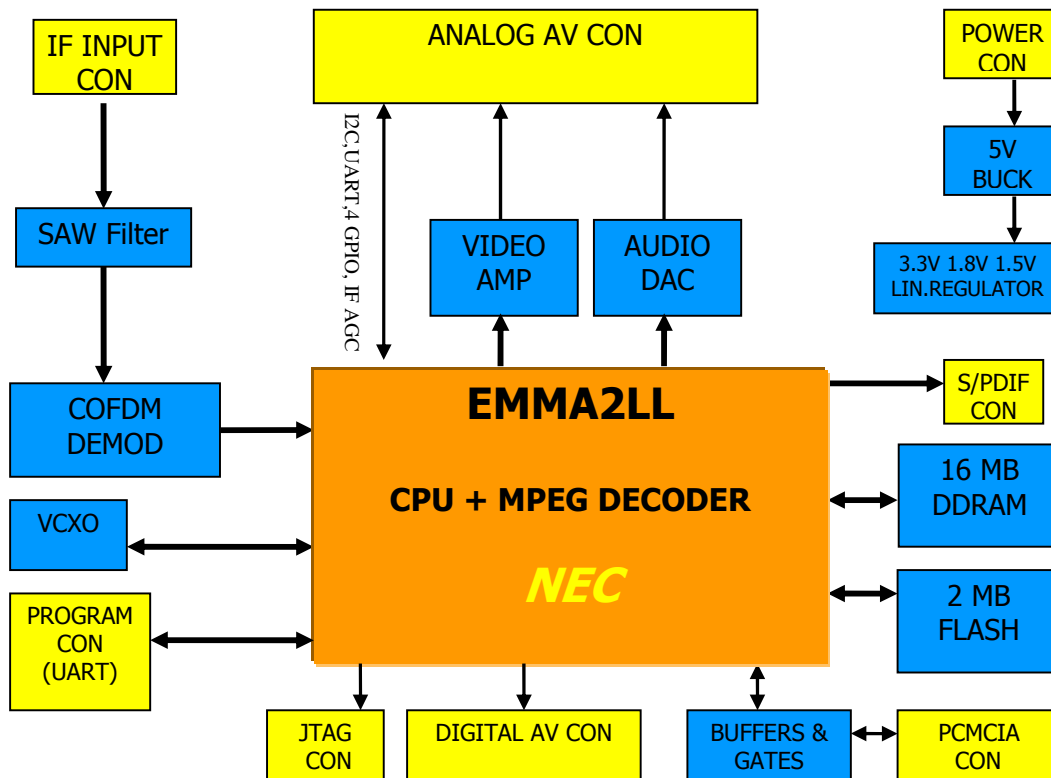
Pin	Signal	Description
1	DVD_Y	DVD Luma Signal
2	DVD_C	DVD Chroma Signal
3	Gnd	Ground

## TDM1300 HARDWARE DESCRIPTION

Item	Description
PCB	4 layer
MPEG decoder	EMMA2LL (NEC)
FLASH	29LV160TE (Spansion, Eon) 2MB
DDRAM	EDD1216AATA ( Elpida, Nanya) 16MB
Audio DAC	CS4335 (Crystal)
Video AMP	FMS6145 (Fairchild)
COFDM Demodulator	DRX3973D (Micronas)
Tuner	DTT7103 (Thomson) DTOS401TH17XA (Samsung)
VCXO	PI6CX100-27 (Pericom)
Buck Regulator	MP1593 (MPS)
3.3V Regulator	NCP1117-3.3V (Onsemi)
1.8V Regulator	NCP1117-1.8V (Onsemi)
1.5V Regulator	NCP1117-1.5V (Onsemi)
74LVC16244 (x4)	16 bit buffer with OE (Various)
74LVC245	Octal Bus Transceiver (Various)
74LVC00	NAND Gate (Various)



## IDTV MODULE BLOCK DIAGRAM



## CONNECTORS

### 1.1 POWER Connector:

Pin	Description
1	+12/24V
2	+12/24V
3	GND
4	GND

### 1.2 EMMA2LL JTAG Connector:

Pin	Description
1	GND
2	JTCLK
3	3.3V
4	JTDO
5	NC
6	JTMS
7	NC
8	JTRST
9	GND
10	JTDI

### 1.3 ANALOG AV Connector:

Pin	Description	Pin	Description
1	DVB_SCL	13	GND
2	DVB_SDA	14	GND
3	GND	15	DVB_R_AUDIO
4	GND	16	DVB_L_AUDIO
5	IRQ	17	GND
6	DVB_RX	18	DVB_IN_CVBS
7	DVB_TX	19	GND
8	GPIO4	20	DVB_IN_B / DVB_IN_C
9	GPIO3	21	GND
10	GPIO2	22	DVB_IN_G / DVB_IN_Y
11	GPIO1	23	GND
12	IF_AGC_DVB	24	DVB_IN_R

#### 1.4 IF Connector:

Pin	Description
1	IF +
2	IF -
3	GND

#### 1.5 PROGRAMMING Connector:

Pin	Description
1	TXD
2	GND
3	RXD

#### 1.6 S/PDIF Connector:

Pin	Description
1	S/PDIF
2	GND

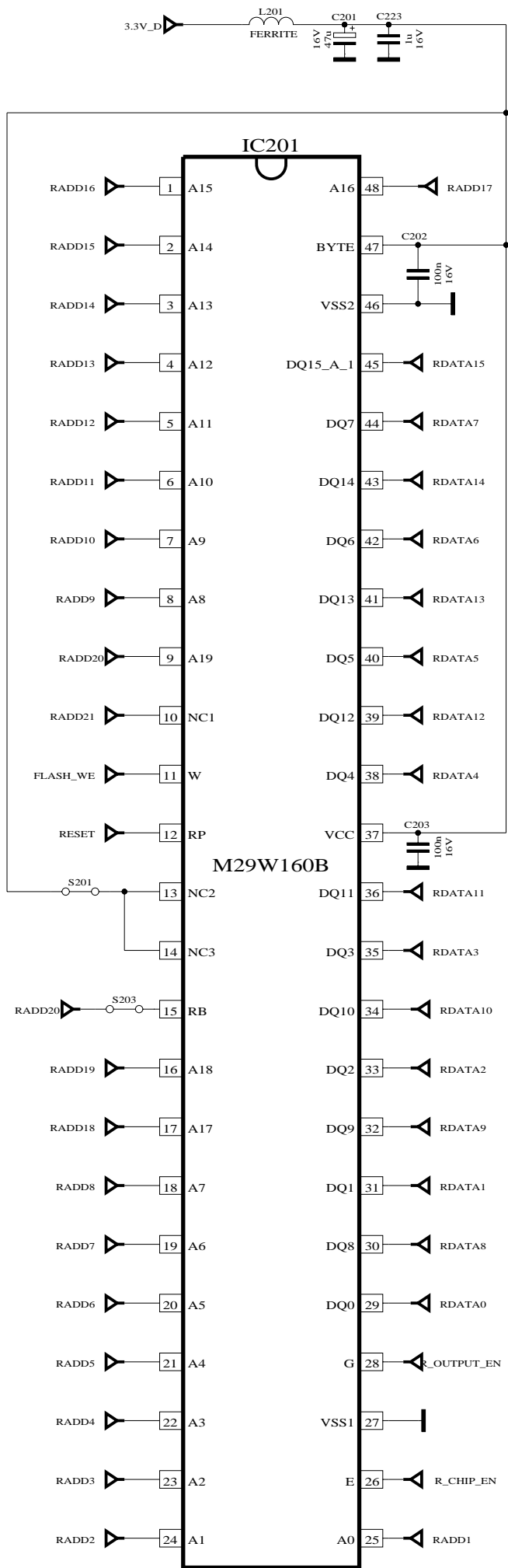
#### 1.7 DIGITAL AV Connector:

Pin	Description	Pin	Description
1	I2S Word Select	11	GND
2	I2S Serial Clock	12	Digital Video Pixel Clock
3	I2S Serial Data	13	Digital Video Y/Cb/Cr DATA7
4	GND	14	Digital Video Y/Cb/Cr DATA6
5	GND	15	Digital Video Y/Cb/Cr DATA5
6	GND	16	Digital Video Y/Cb/Cr DATA4
7	Internal Vertical SYNC	17	Digital Video Y/Cb/Cr DATA3
8	Internal Horizontal SYNC	18	Digital Video Y/Cb/Cr DATA2
9	GND	19	Digital Video Y/Cb/Cr DATA1
10	GND	20	Digital Video Y/Cb/Cr DATA0

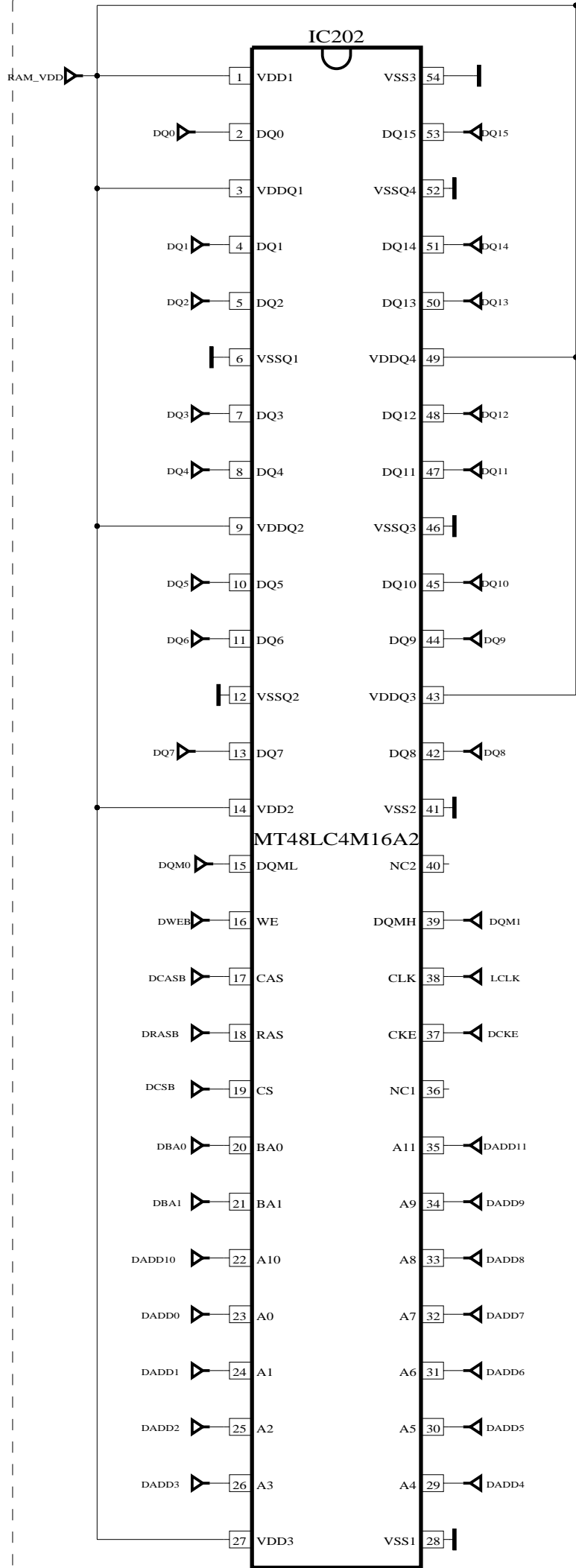
## 1.8 PCMCIA Connector:

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground	35	GND	Ground
2	D3	Data bit 3	36	CD1#	Card Detect
3	D4	Data bit 4	37	MDO3	MPEG Data Out 3
4	D5	Data bit 5	38	MDO4	MPEG Data Out 4
5	D6	Data bit 6	39	MDO5	MPEG Data Out 5
6	D7	Data bit 7	40	MDO6	MPEG Data Out 6
7	CE1#	Card Enable	41	MDO7	MPEG Data Out 7
8	A10	Address bit 10	42	CE2#	Card Enable
9	OE#	Output Enable	43	VS1#	Voltage Sense 1
10	A11	Address bit 11	44	IORD#	I/O Read
11	A9	Address bit 9	45	IOWR#	I/O Write
12	A8	Address bit 8	46	MISTR#	MPEG Data In Start
13	A13	Address bit 13	47	MDI0	MPEG Data In 0
14	A14	Address bit 14	48	MDI1	MPEG Data In 1
15	WE#	Write Enable	49	MDI2	MPEG Data In 2
16	IREQ#	Interrupt Request	50	MDI3	MPEG Data In 3
17	VCC	Supply Voltage	51	VCC	Supply Voltage
18	VPP	Programming and Peripheral Supply	52	VPP	Programming and Peripheral Supply
19	MI VAL	MPEG Data In Valid	53	MDI4	MPEG Data In 4
20	MCLKI	MPEG Data Clock Input	54	MDI5	MPEG Data In 5
21	A12	Address bit 12	55	MDI6	MPEG Data In 6
22	A7	Address bit 7	56	MDI7	MPEG Data In 7
23	A6	Address bit 6	57	MCLKO	MPEG Data Clock Output
24	A5	Address bit 5	58	RESET	Card Reset
25	A4	Address bit 4	59	WAIT#	Extend bus cycle
26	A3	Address bit 3	60	INPACK#	Input Port Acknowledge
27	A2	Address bit 2	61	REG#	Register select & I/O Enable
28	A1	Address bit 1	62	MO VAL	MPEG Data Out Valid
29	A0	Address bit 0	63	MOSTRT	MPEG Data Out Start
30	D0	Data bit 0	64	MDO0	MPEG Data Out 0
31	D1	Data bit 1	65	MDO1	MPEG Data Out 1
32	D2	Data bit 2	66	MDO2	MPEG Data Out 2
33	IOIS16#	I/O Port Is 16-bit	67	CD2#	Card Detect
34	GND	Ground	68	GND	Ground

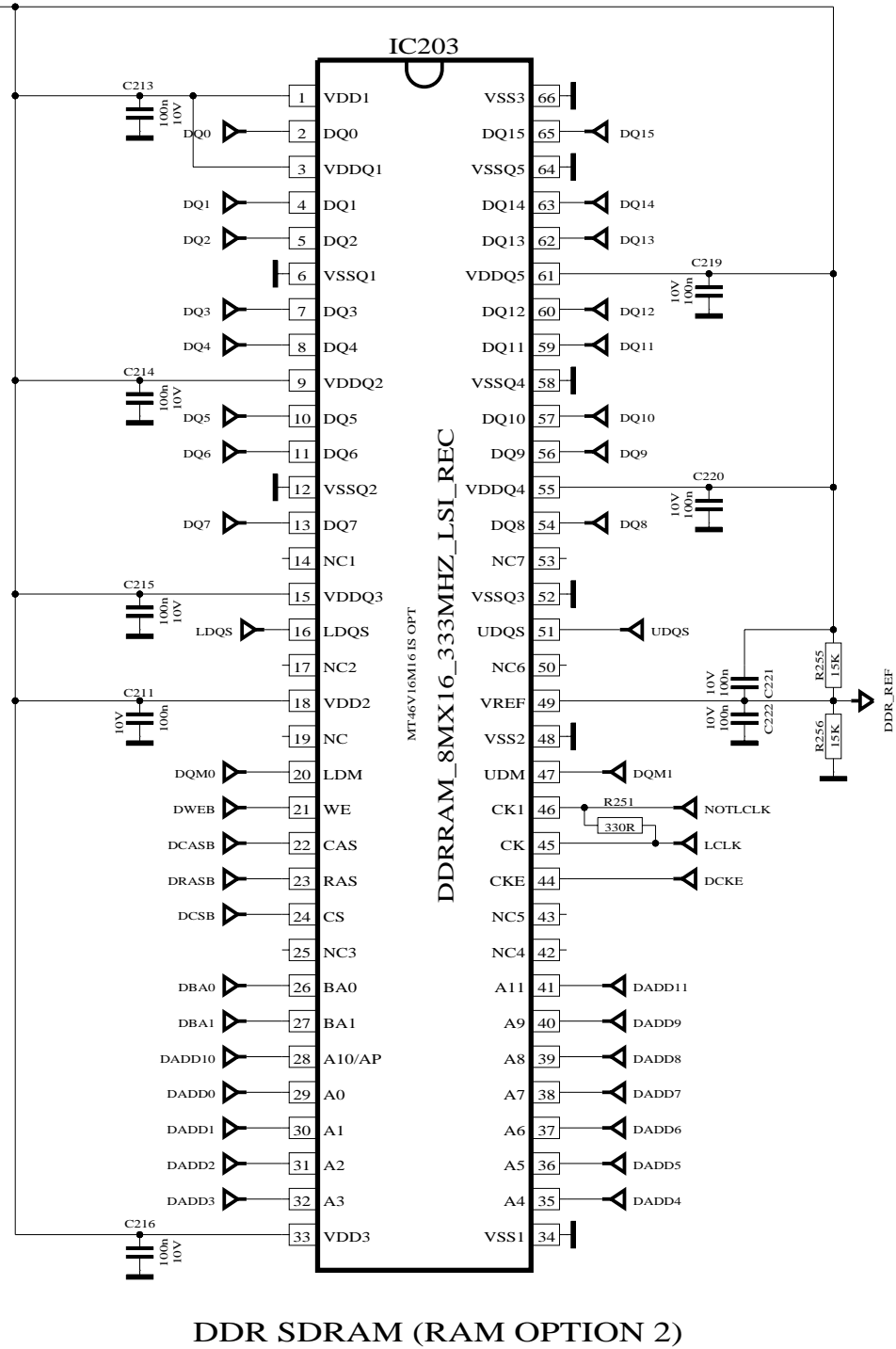




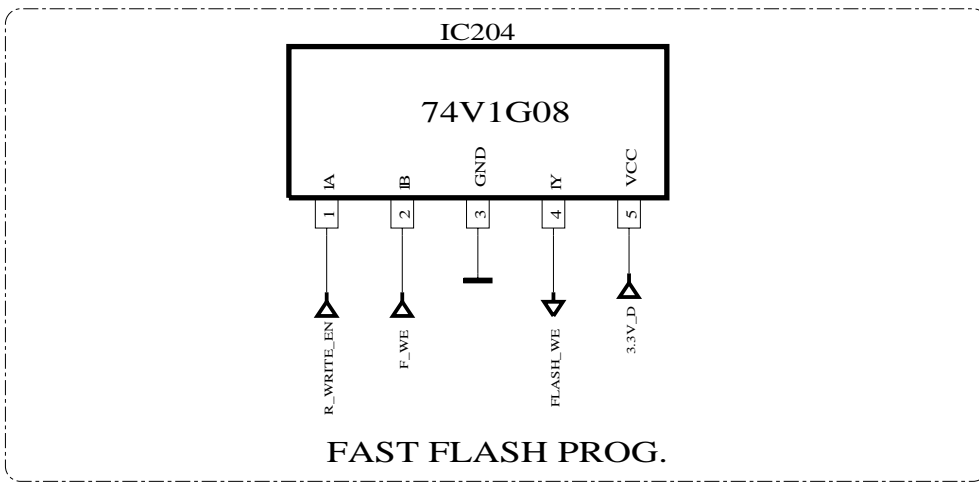
FLASH ROM

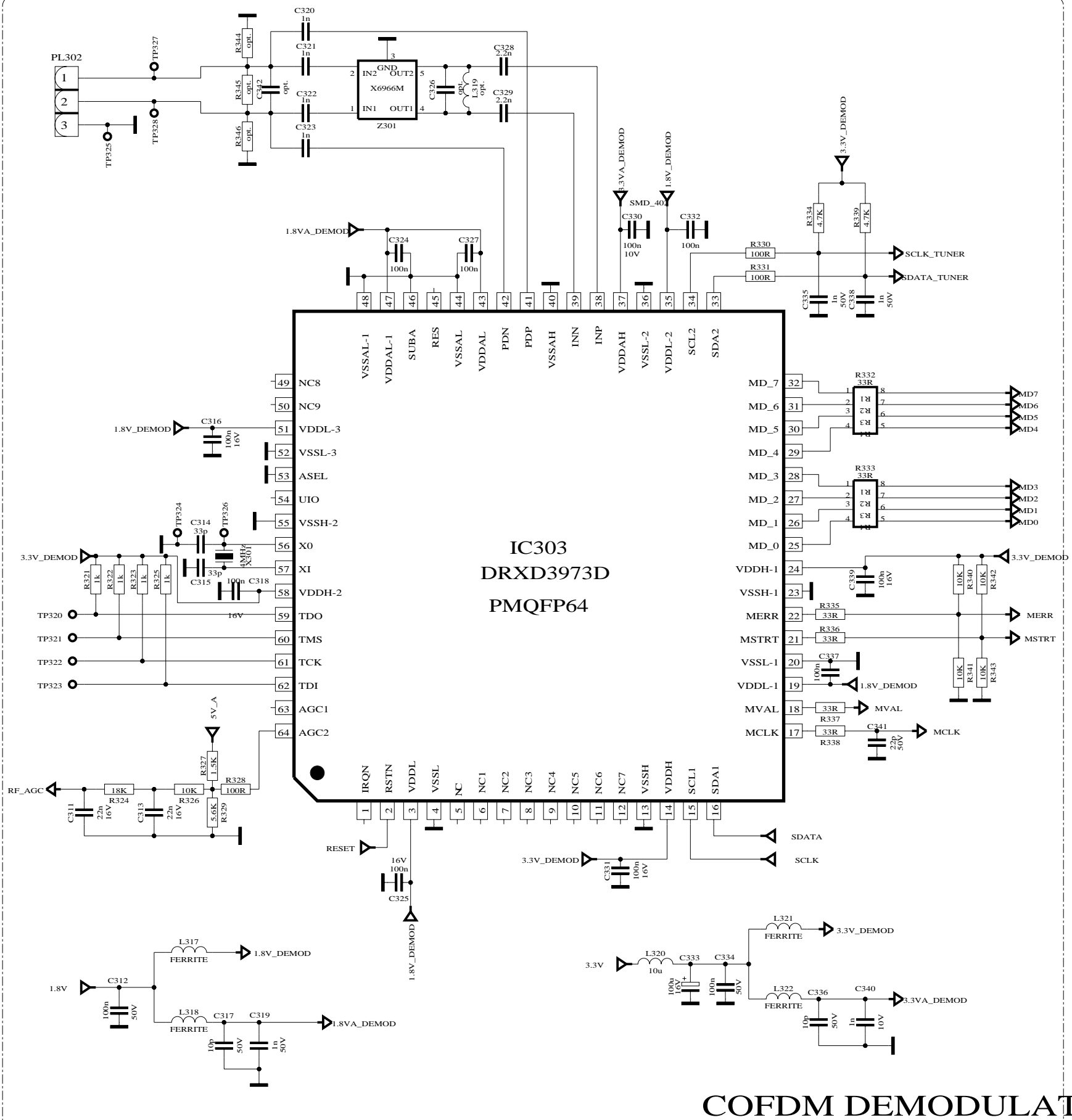
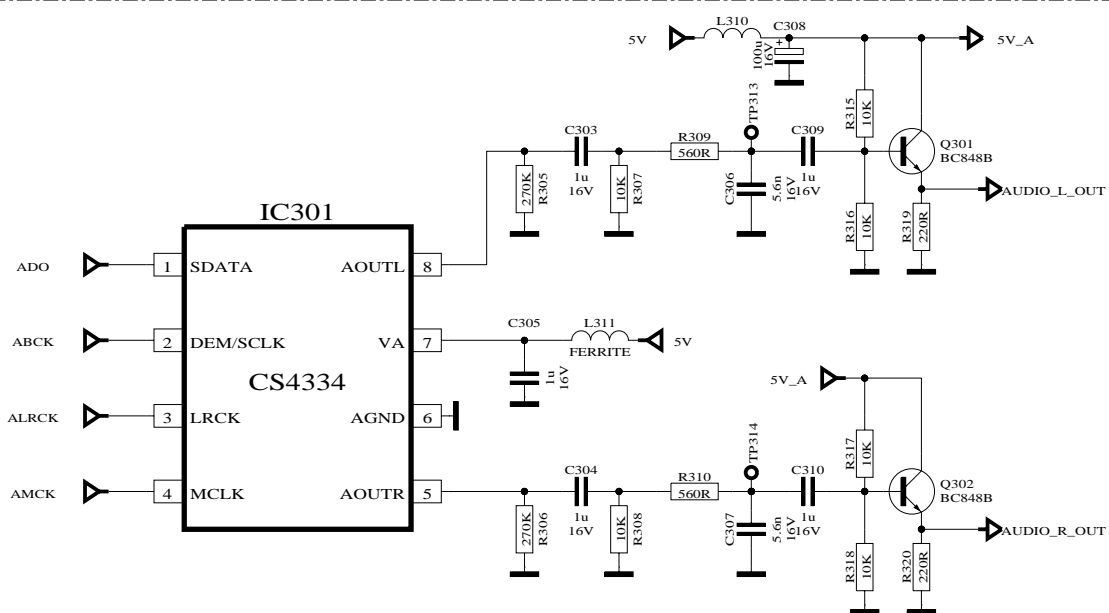
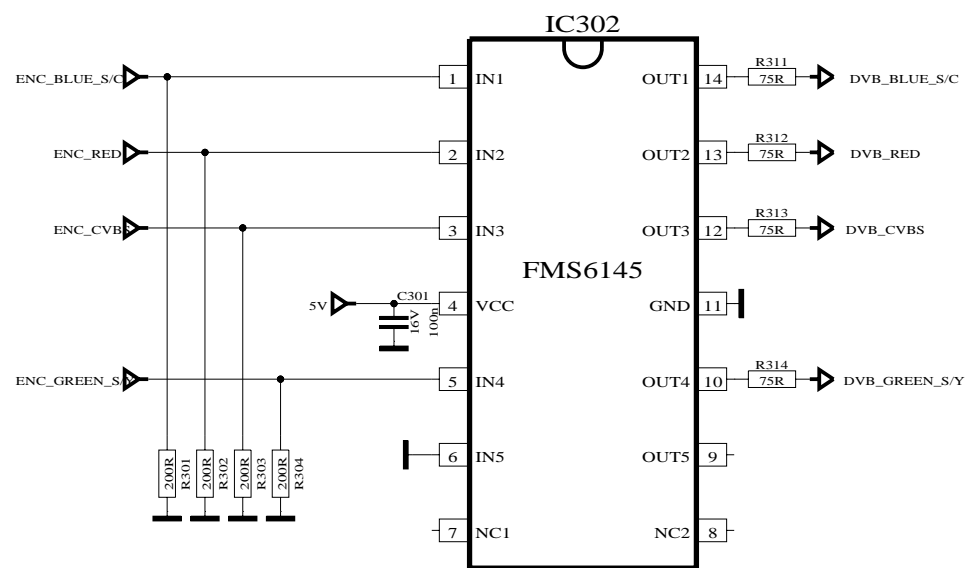
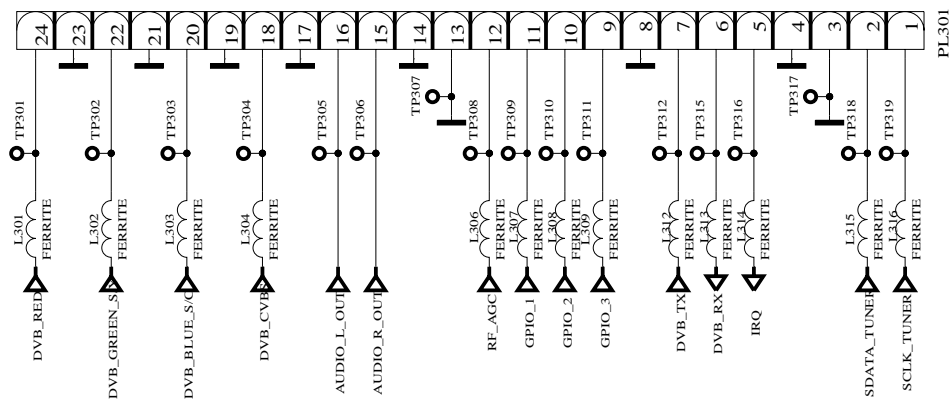


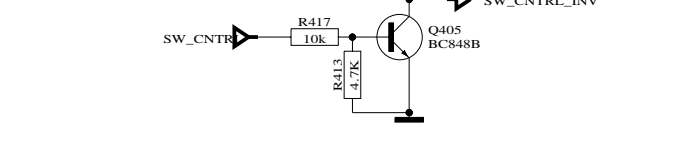
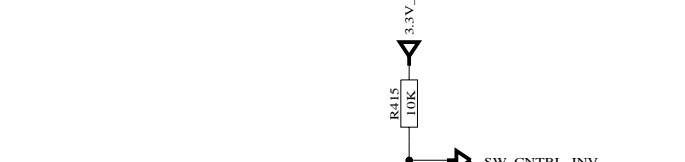
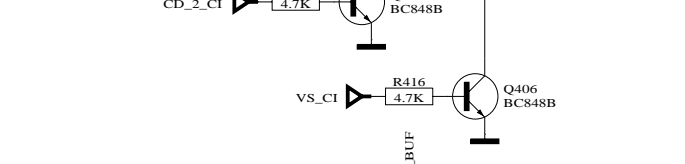
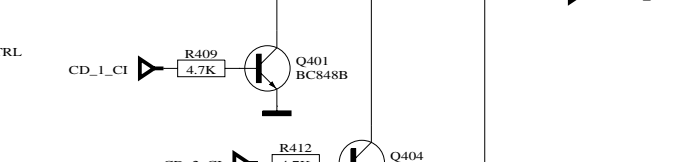
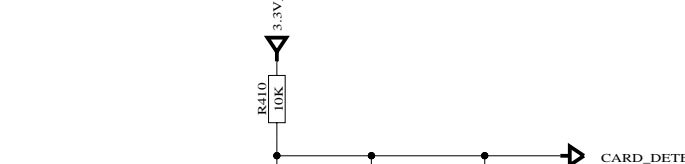
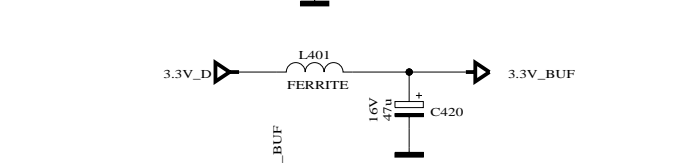
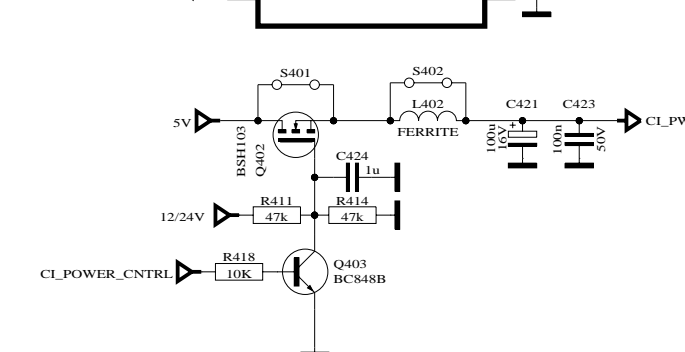
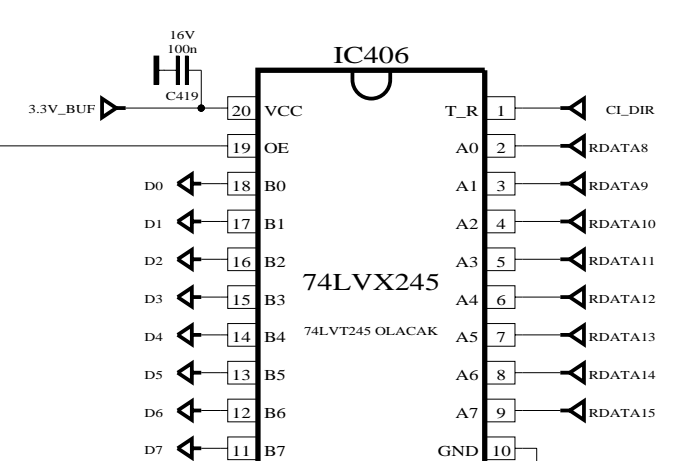
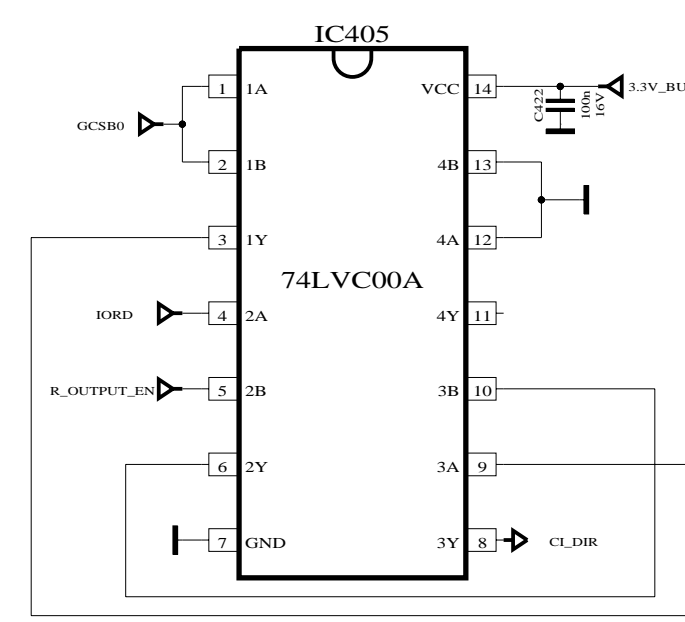
SDRAM (RAM OPTION 1)



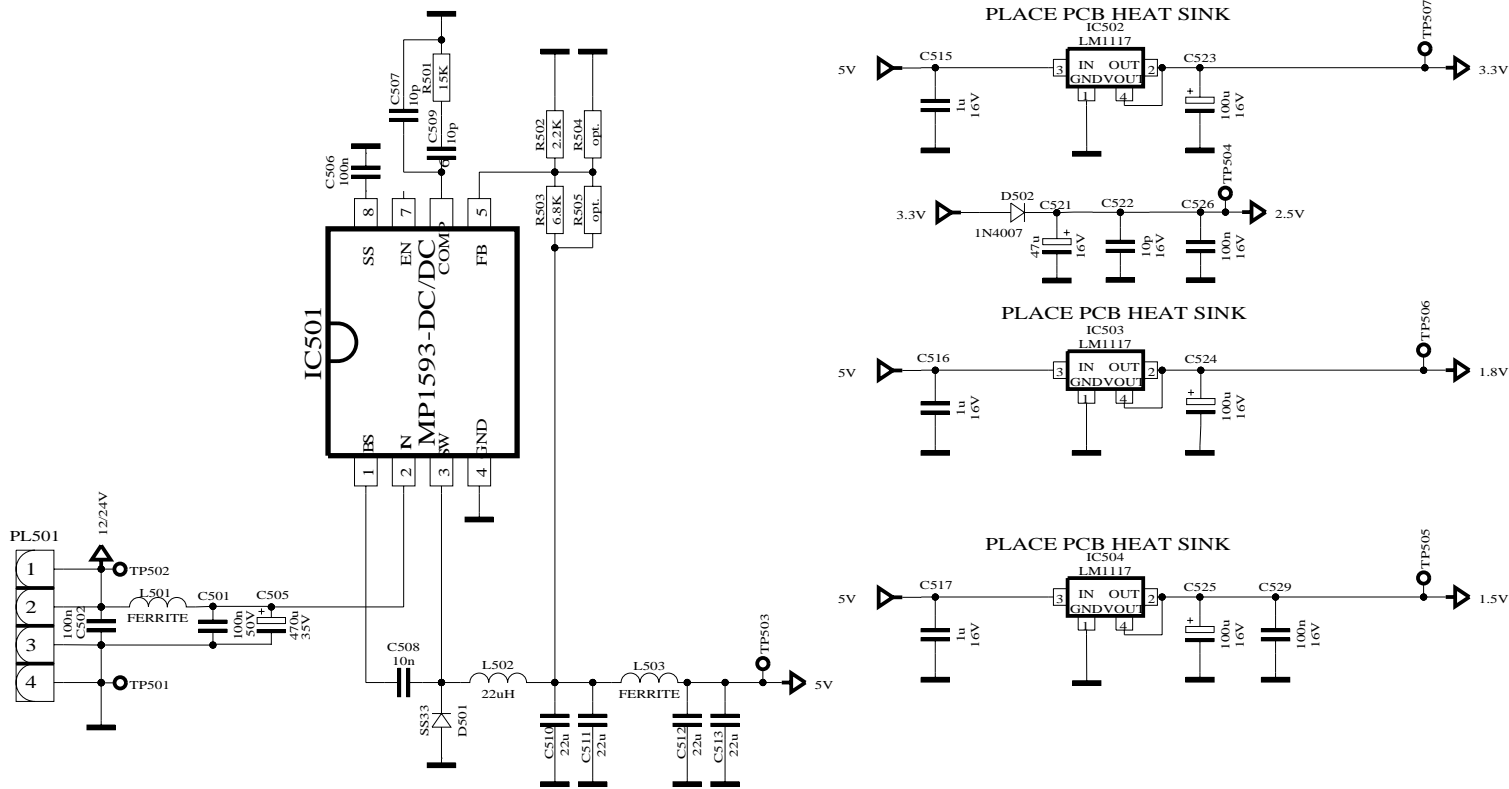
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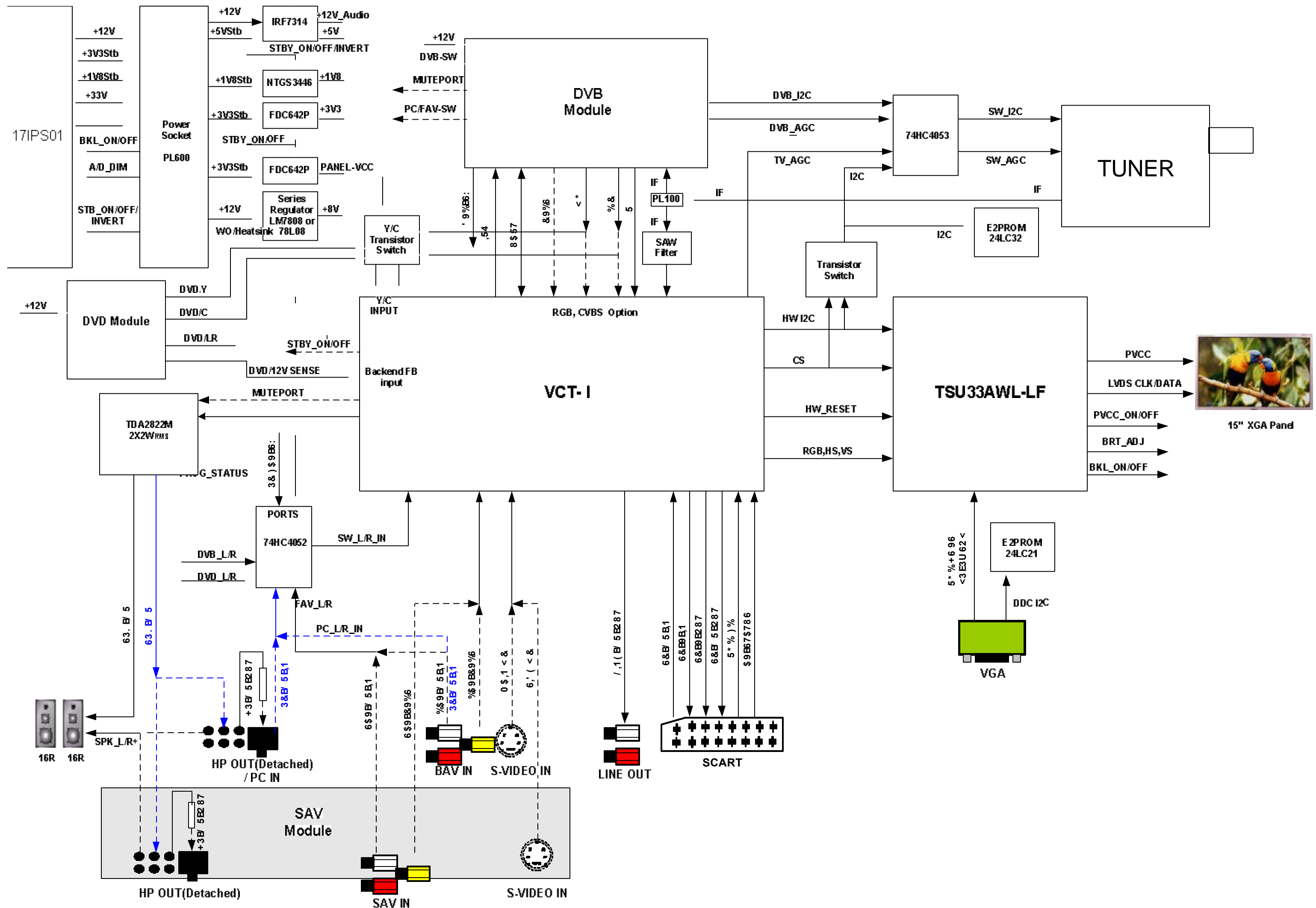


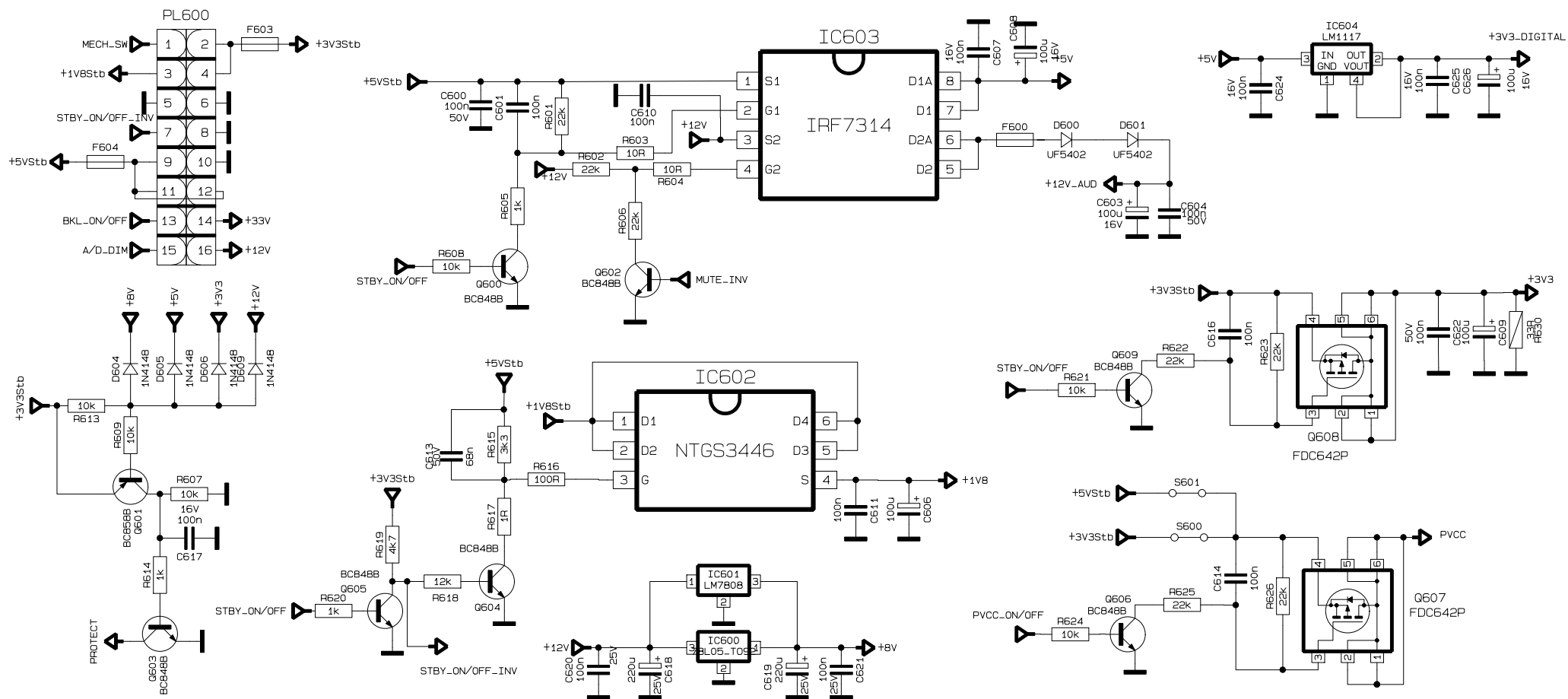


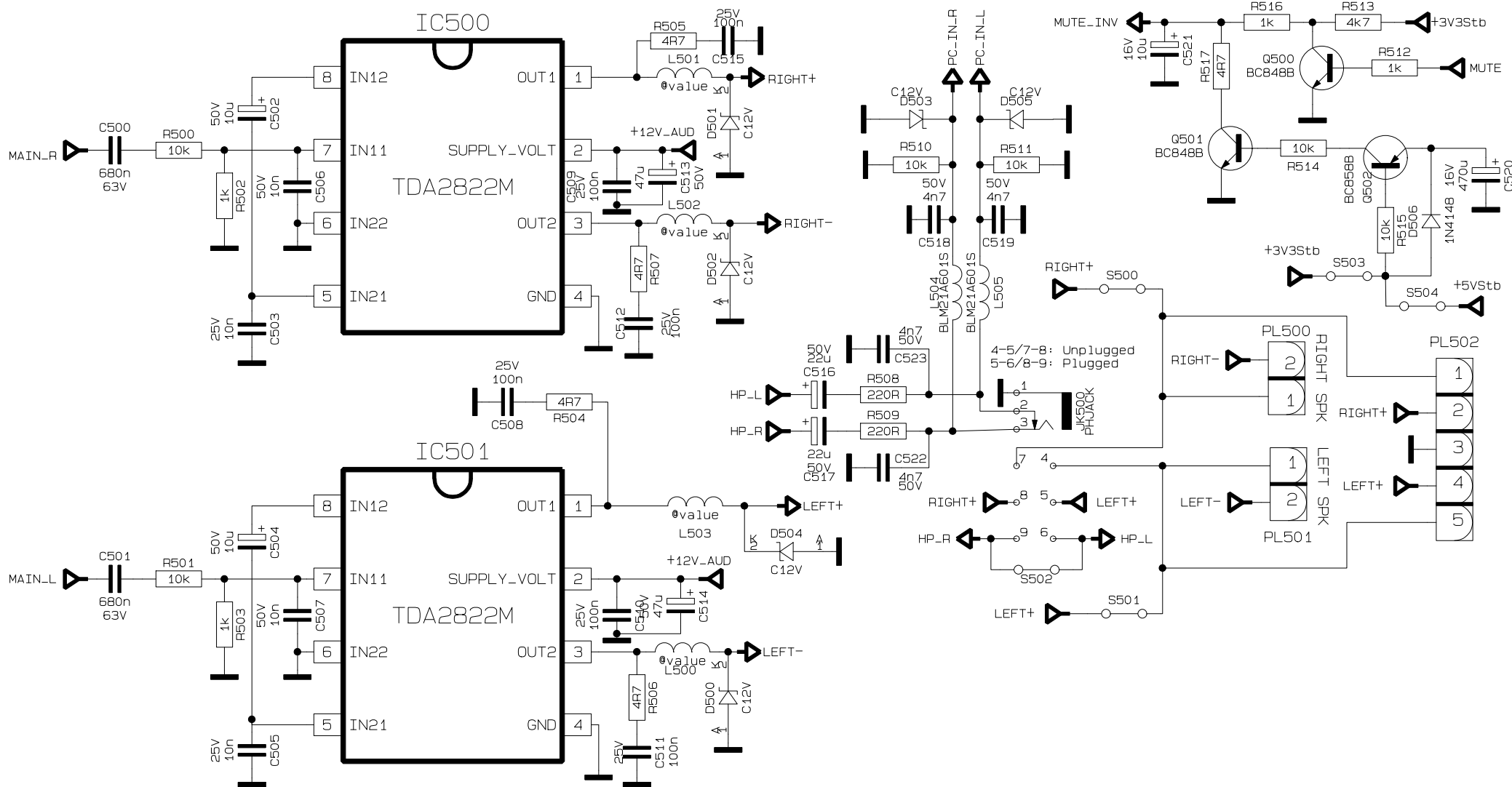


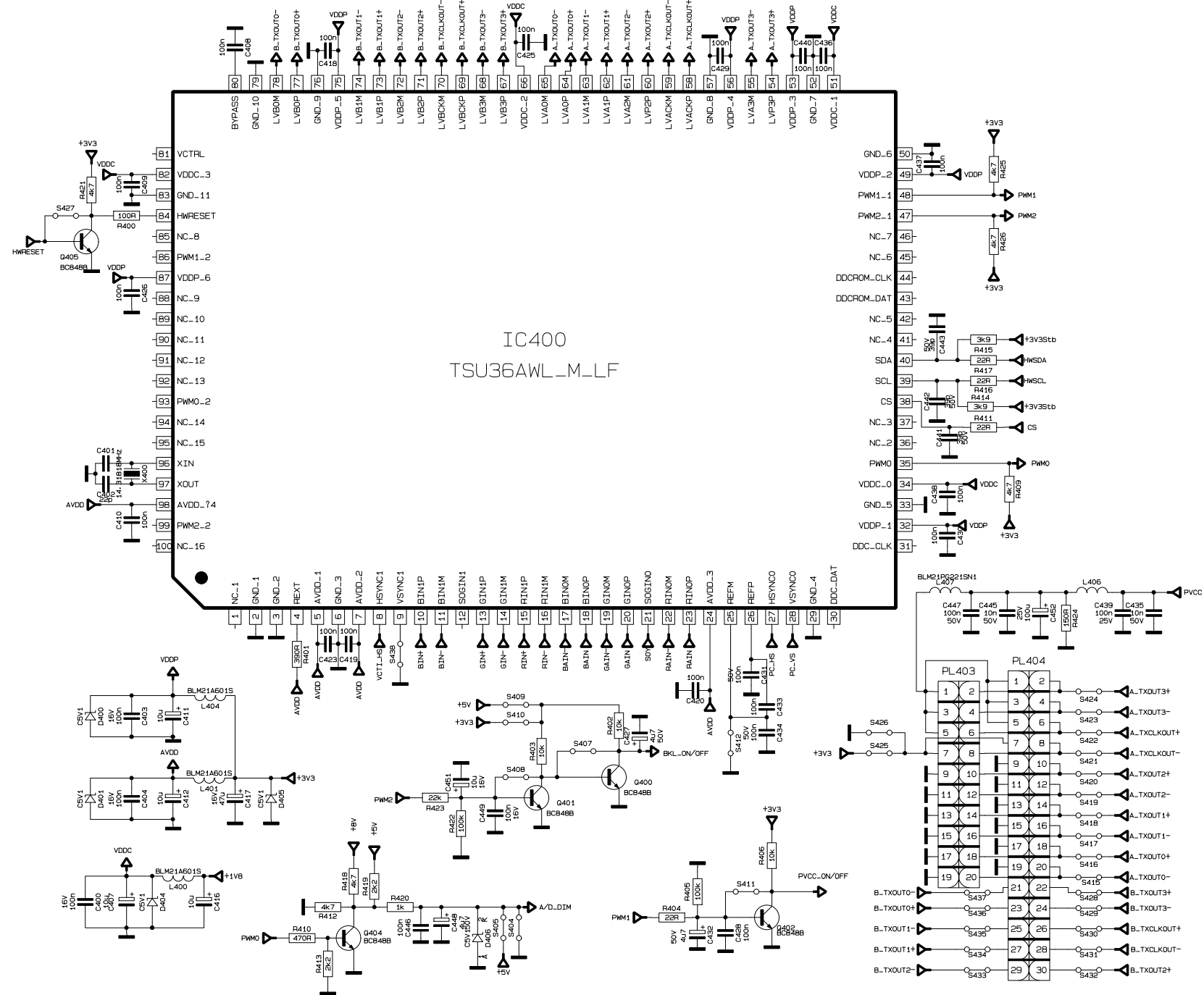


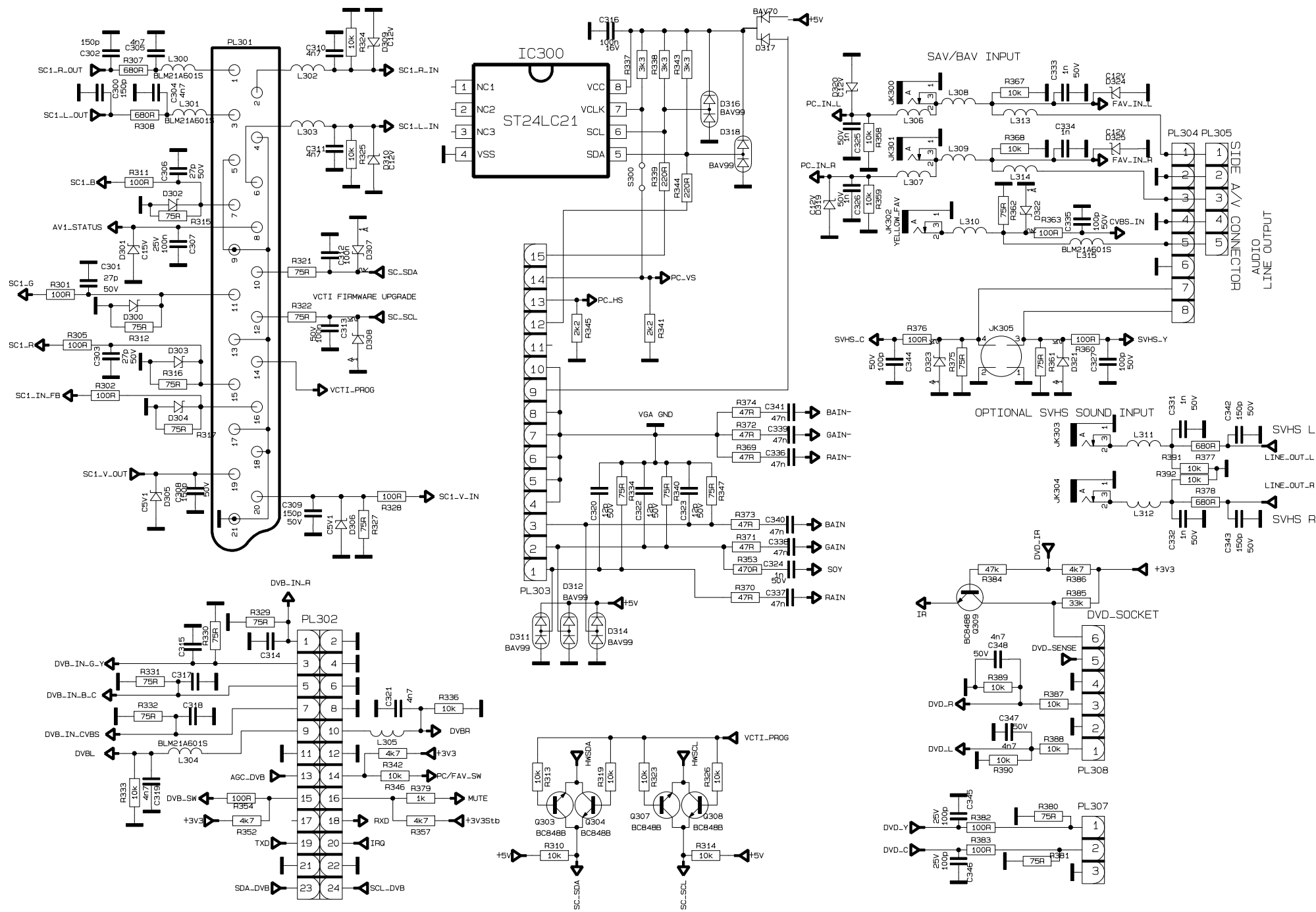
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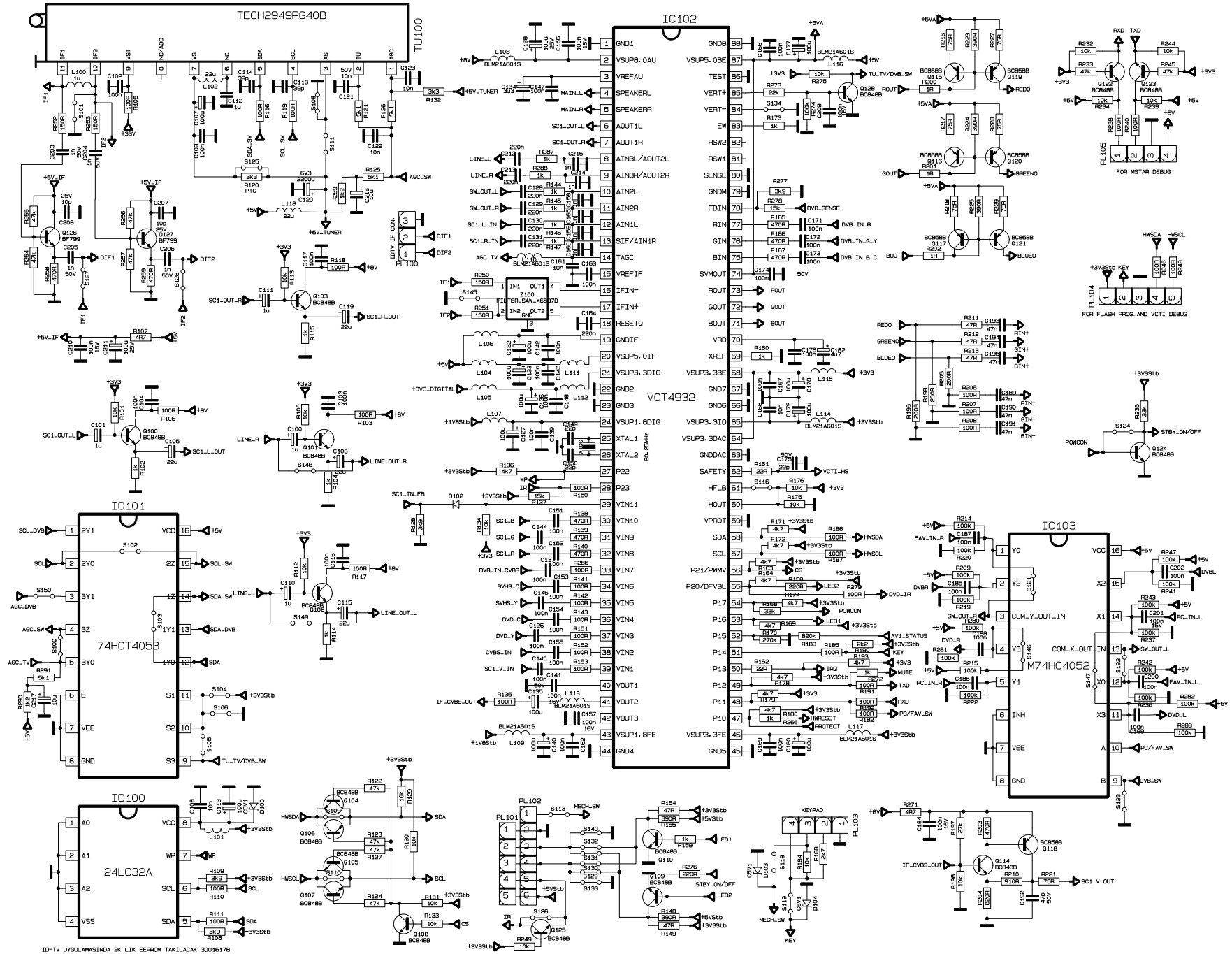


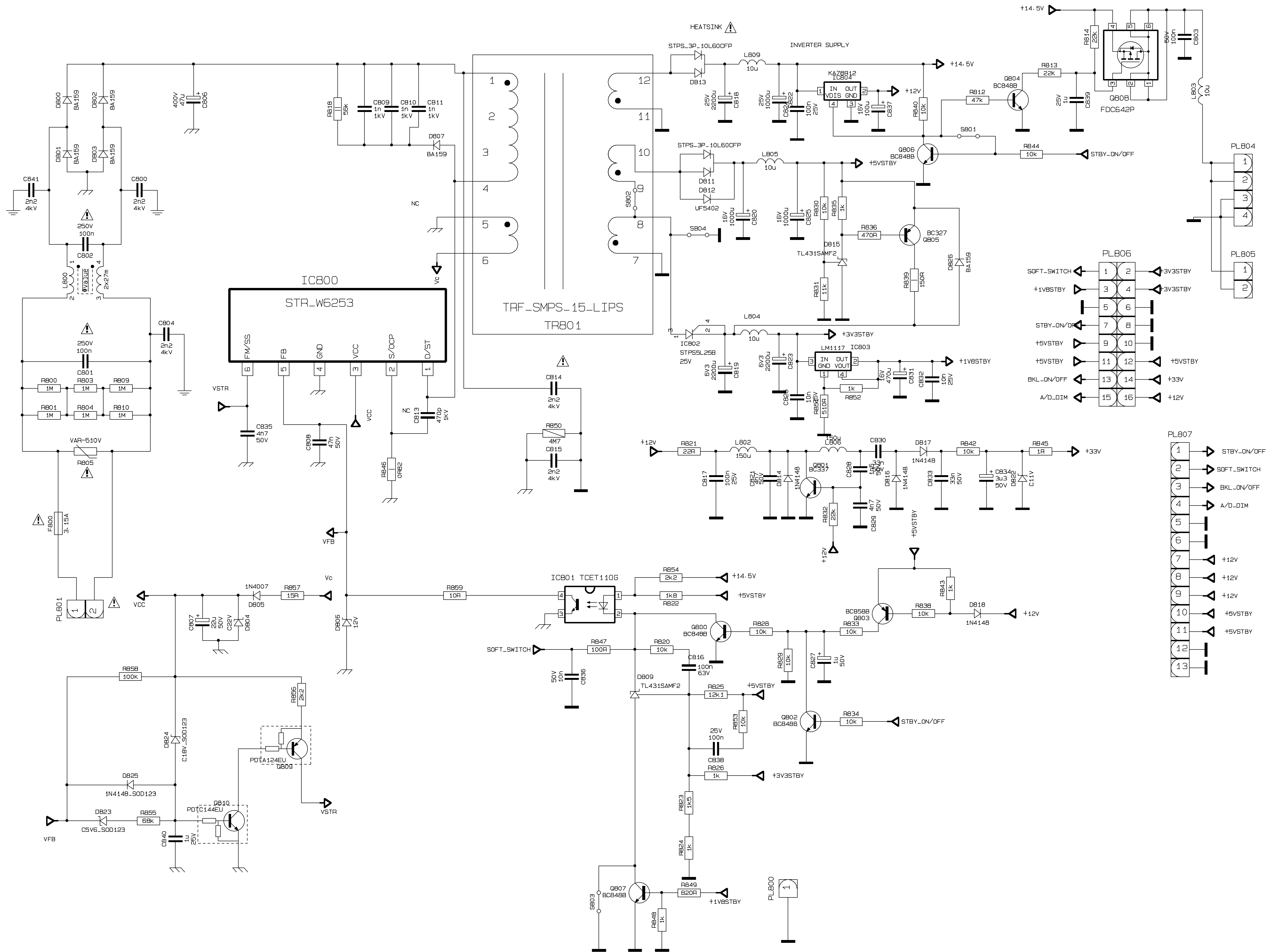




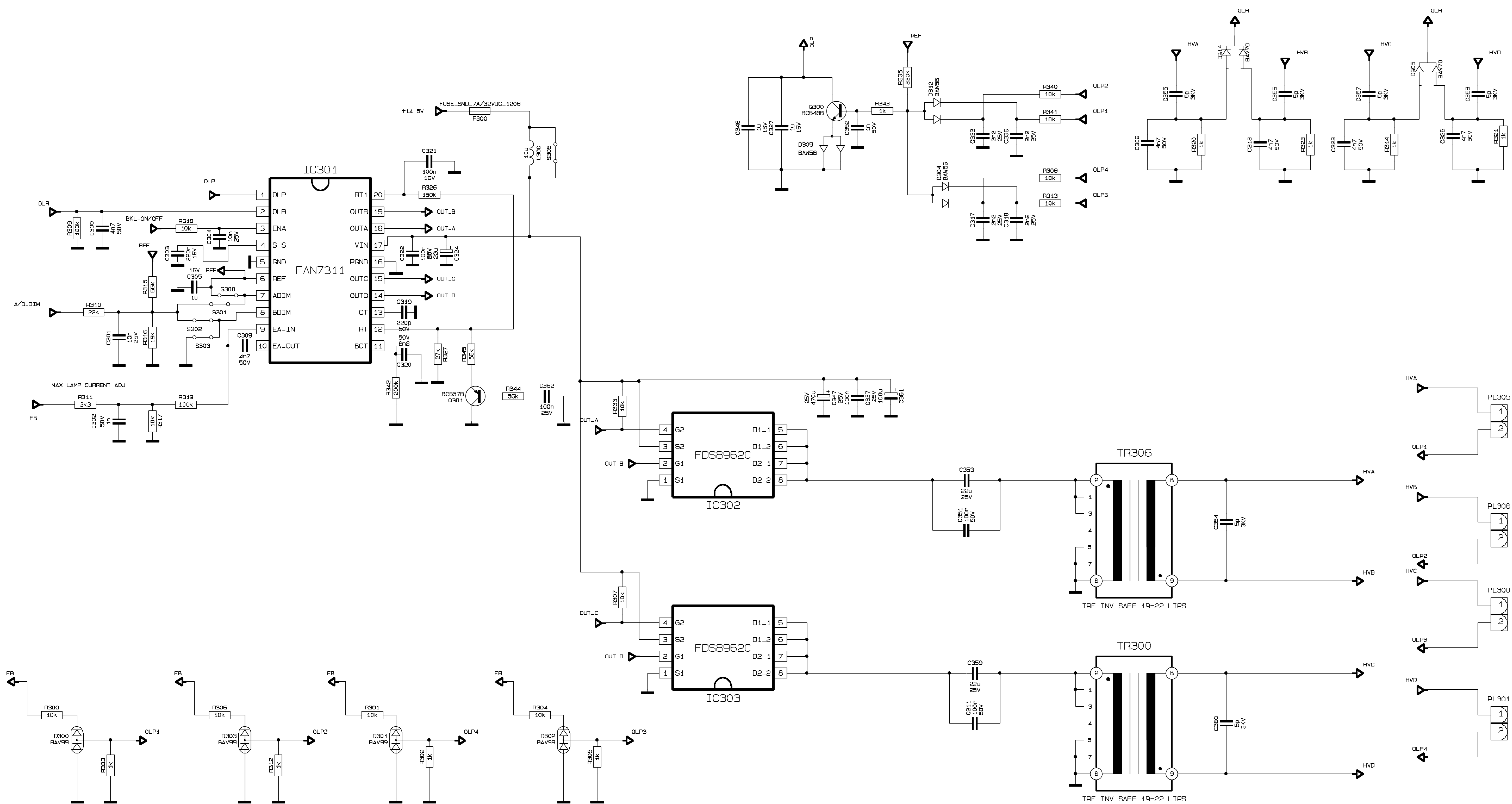












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